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SPECIFICATION

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FSP1200-50DRS

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SPECIFICATION

FSP1200-50DRS

2U 1200W Redundant Power Supply

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1 REVISION LOG

This section contains the release history of this document:

Date	Revision	Section	Issue
2012/08/10	0.1		
2012/11/16	0.2	3.1.8	Update Efficiency
2013/08/23	0.3	3.2.2	Revise +5Vsb Output rating
2013/08/27	0.4	3.1.3	Add HVDC Input Voltage specification
2014/01/13	0.5	6	Add Smart On Function
2014/08/08	0.6	11	Revise 11. PSMC Interface
2014/09/02	0.7	11.2.7 11.2.11	Revise STATUS_VOUT Command Revise STATUS_FAN_1_2 Command
2014/11/28	0.8	11.4	Revise Firmware Protection-Over Temperature(Module)

APPROVE	Jerry Tsai	CHECK	Brian Chen	PREPARE	Chang Bo Liu

2 GENERAL SCOPE

This specification describes the performance characteristic of a 1200W AC-DC switching redundant power supply. The power supply shall be able to operate as a single supply, or in a 1+1 parallel hot-plug able operation with active load sharing in a 1+1 redundant configuration.

2.1 Mechanical Overview

The physical size of the power supply enclosure is intended to accommodate the power range of up to 1200W. The physical size is 84mm x 76mm x 330mm (height x width x length).

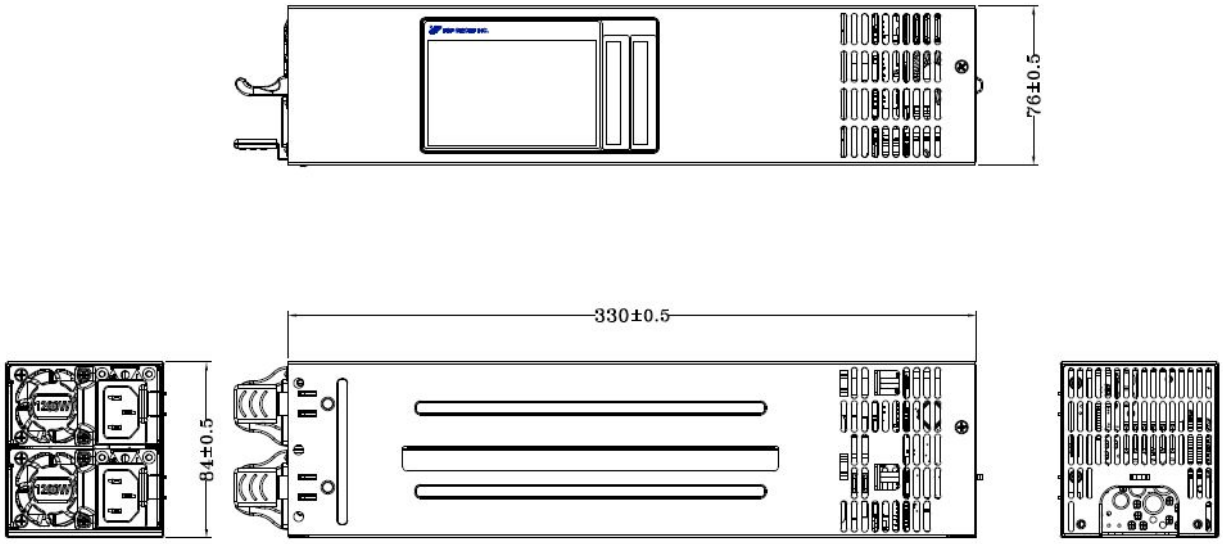


Figure 1 – Power Supply Dimension

2.2 LED Marking and Identification

The power supply shall have two LED for indication of the power supply status.

Table 1 – LED Status Information

Power supply condition	Power supply LED
No AC power to all PSU	OFF
AC present/only standby output on	1Hz Flashing Blue
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	Red
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Red
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	Red

NOTE: * Flashing frequency: 1Hz (0.5 sec Red/ 0.5sec Blue)

2.3 Environmental Requirements

The power supply shall operate within all specified limits over specified conditions in 2.3.

The defined operation condition include temperature, humidity, altitude, shock and vibration.

2.3.1 Temperature and Humidity Requirements

The power supply shall operate within all specified limits over T_{op} temperature range and specified humidity Range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

The power supply shall withstand thermal storage specified in $T_{non\text{-}OP}$ without any damage.

Table 2 – Temperature Requirements

Item	Description	MIN	MAX	Unit
T_{OP}	Operating temperature range.	0	50	°C
$T_{non\text{-}OP}$	Non-Operating temperature range.	-40	70	°C
H_{OP}	Operating humidity range, non-condensing		90	%
$H_{non\text{-}OP}$	Non-Operating humidity range, non-condensing		95	%

2.3.2 Altitude Requirements

The power supply shall operate within all specified limits over A_{op} Altitude range. The change pressure condition shall not harm the power supply and the operation within specified regulations shall be assured.

The power supply shall withstand Altitude storage specified in $A_{non\text{-}OP}$ without any damage.

Table 3 – Altitude Requirements

Item	Description	MIN	MAX	Unit
A_{OP}	Operating Altitude range.	0	5000	m
$A_{non\text{-}OP}$	Non-Operating Altitude range.	0	15000	m

3 ELECTRICAL PERFORMANCE

3.1 AC power Input Specification

3.1.1 AC Inlet connector

The power supply shall incorporate an AC input connector complying to IEC 320 C-14 power inlet connector specification. This inlet shall be rated for operation at 15A/250VAC.

3.1.2 Input voltage and frequency specification

The power supply shall operate within all specified limits over the following input range. Harmonic distortions of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits.

The power supply shall power off if the AC input is below VAC_{low_limit} and shall start (auto recover) if $VAC_{recover}$ is reached. Input of VAC below $VAC_{recover}$ shall not cause any damage to the power supply, including the input fuse.

Table 4 – Rated output power for each input voltage range

Parameter	Minimum input	Rated Input	Maximum input
115VAC	90 V_{rms}	100-127 V_{rms}	140 V_{rms}
230 VAC	180V_{rms}	200-240V_{rms}	264V_{rms}
Frequency	47Hz	50/60Hz	63Hz

3.1.3 HVDC Input voltage

The power supply supports High Voltage Direct Current (HVDC) input. Allowed HVDC input range as shown in below table. The power supply shall operate within all specified limits, when HVDC input meet requirements defined in this chapter.

Table 5 – HVDC input voltage range

Parameter	Minimum input	Rated Input	Maximum input
HVDC(240)	180V	240V	264V

3.1.4 Input current

The maximum input current defines the maximum possible input current to ensure the proper function of the power supply to meet all defined specifications.

Table 6 – Maximum input current

Input voltage	Input current	Max power
90-140VAC	12A	900W
180-264VAC	9A	1200W
240Vdc	6A	1200W

3.1.5 AC Line Fuse

The power supply shall incorporate one input fuse on the line side for input over-current protection to prevent damage to the power supply and meet product safety requirements. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.1.6 AC line inrush

The maximum AC line inrush current shall be 80A peak at an input voltage of 264VAC.
Inrush current shall be measured at an ambient temperature of 25 deg C after the input voltage has been removed from the power supply for a minimum of 10 minutes.

3.1.7 Input Power Factor Correction

The input Power Factor shall be greater than 0.98/115Vac and 0.96/230Vac (show the below Table 7.)

Table 7 – Power Factor Correction

Input voltage	Below 10% loading	Below 50% loading	100% loading
115VAC/60Hz	>0.8	>0.95	0.98
230VAC/50Hz	>0.8	>0.95	0.96

3.1.8 AC line dropout

An AC line dropout is a transient condition defined as the AC input to the power supply drops to 0 VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulations requirements. An AC line dropout of any duration shall not cause dripping of the control signals and protection circuits. If the AC dropout lasts longer than the holdup time, the power supply should recover when VAC meets $VAC_{recover}$ and meet all turn on requirements.
A Input dropout of any length shall not cause any damage to the power supply.

Table 8 – Hold-up time until Power output goes out of regulations

Loading	Main output	Standby output
100%	12mS	70mS

3.1.9 Efficiency

The redundant power supply module efficiency should meet at least Climate Saver 3 / 80Plus Platinum rating, specified in below table. The efficiency should be measured at 230VAC and with external fan power according to Climate Saver / 80Plus efficiency measurement specifications (CSCI-09-10)

Table 9 – module efficiency requirements

Efficiency Std.	20% load	50% load	100% load
Platinum	90%	94%	91%

3.1.10 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 10 – Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec. limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.1.10.1 Electrical Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024:1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.1.10.2 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-4:1995 test standard and performance criteria B define in Annex B of CISPR 24.

3.1.10.3 Radiated Immunity

The power supply shall comply with the limits defined in EN55024:1998 using the IEC61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

3.1.10.4 Surge Immunity

The power supply shall be tested with the system for immunity to AC Ringwave and AC Unidirectional wave, both up to 2kV, per EN55024:1998, EN 61000-4-5:1995 and ANSI C62.45:1992.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B f CISPR 24.

3.1.10.5 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions.

“Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions.

“Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 11 – AC Line SAG transient performance.

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC voltage**	**Line frequency**	**Performance criteria**
0 to 1/2 AC cycle	95%	Nominal AC voltage	50/60Hz	No loss of function or performance
>1 AC cycles	>30%	Nominal AC voltage	50/60Hz	Loss of function acceptable, self-recoverable

Table 12 – AC Line SURGE transient performance.

AC Line Surge				
Duration	**Surge**	**Operating ac voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	Mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

3.1.10.6 AC line fast transient (EFT) specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.1.11 Power Recovery

The power supply shall recover automatically (auto recover) after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.1.12 Voltage Brown Out

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

In addition the power supply shall meet the following requirements:

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply must be able to return to normal power up state after a brownout (Sag) condition. During brownout test from 120VAC to 0VAC @ 900W with 3mins ramp, input current shall never exceed fuse and shall not blow the fuse.

3.1.13 AC Line Leakage Current

The maximum leakage current to ground for each power supply shall be 3.5mA when tested at 240VAC/50Hz.

3.2 DC output voltages

3.2.1 Grounding

The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 100mΩ (Test Conditions 40A for 120sec). This path may be used to carry DC-current.

3.2.2 Output rating

The following table defines the power and current rating of the power supply. The combined output power of all outputs shall not exceed the rated output power. The power supply must meet both static and dynamic voltage regulation requirements.

Table 13 – Output Power and Current Ratings

Output	Minimum Current(A)	Maximum Current(A)	Output Power(W)	
+12V	0.5	72.6 for 90~180Vrms 97.6 for 180~264Vrms	871W for 90~180Vrms 1171W for180~264Vrms	900W for 90~180Vrms 1200W for180~264Vrms
+5V	0	30	180W	
+3.3V	0	30		
-12	0	0.3	3.6W	
+5Vsb	0	5	25W	

3.2.3 Auxiliary Output (Standby)

The 5Vsb output shall be present when an AC input greater than $V_{recover}$ is applied.

3.2.4 No load operation

The power supply shall meet all requirements except for the transient loading requirements when operated at no load on all outputs.

3.2.5 Voltage Regulation

The power supply shall meet the Voltage regulation under all operating conditions (AC line, transient loading, output loading). These limits include the peak-peak ripple/noise. The regulation of Table 14 shall be measured at the output connector of the power supply, subject to the dynamic loading conditions in paragraph 3.2.7.

Table 14 – Output Voltage regulation

Output	Minimum	Nominal	Maximum	Unit
+12V	11.4	12.0	12.6	Vdc
+5V	4.75	5.0	5.25	Vdc
+3.3V	3.135	3.3	3.465	Vdc
-12V	11.40	12.0	12.6	Vdc
+5Vsb	4.75	5.0	5.25	Vdc

3.2.6 Ripple and Noise Regulation

Ripple and Noise is defined in table 15. Ripple and Noise shall be measured over a Bandwidth of 0Hz to 20MHz at the power supply output connector. A 0.1μF ceramic capacitor and 47μF of tantalum capacitor shall be placed at each point of measurement. The measurement points shall be as close as possible to the point of load.

The ripple and noise specification shall be met over all load ranges and AC line voltages with 1+1 power supplies in parallel operation.

Table 15– Ripple and Noise Regulation

Output	Maximum	Unit
+12V	120	mV
+5V	50	mV
+3.3V	50	mV
-12V	120	mV
+5Vsb	50	mV

3.2.7 Dynamic loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.

The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging . The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load and the MAX load.

This shall be tested with no additional bulk capacitance added to the load.

Table 16 – Transient Load Requirements

Output	Δ Step size	Slew Rate	Capacitive Load
+3.3V	30% OF MAX.	0.5A/μs	2200μF
+5V	30% OF MAX.	0.5A/μs	2200μF
+12V	60% OF MAX.	0.5A/μs	10000μF
+5Vsb	25% OF MAX.	0.5A/μs	100μF

Note: For dynamic conditions +12V min. loading is 1A.

3.2.8 Capacitive load

The power supply shall operate within specifications over the capacitive loading ranges defined below in table 17.

Table 17 – Capacitive Loading Conditions

Output	Min	Max
+3.3V	10μF	12,000μF
+5V	10μF	12,000μF
+12V	10μF	11,000μF
-12V	1μF	350μF
+5Vsb	1μF	350μF

3.2.9 Maximum load change

The power supply shall continue to operate normally when there is a step change ≤ 1 A/μsec. between minimum load and maximum load.

3.2.10 Close loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -12dB-gain margin is required.
Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.2.11 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on/off. The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied.

3.2.12 Soft starting

The power supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load condition.

3.2.13 Hot Swap Requirements

Hot Swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON# asserted, while in standby mode with PSON# de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

Insertion: The power supply may be inserted into the system with PSON# asserted, with PSON# de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general a failed (of by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

3.2.14 Load sharing control

The +12 V output shall have active load sharing. When operating at 50% of full load, the output current of any 1+1 power supplies shall be within (+/-6.5%). For example, if power supply #1 is operating at 20A, then all other power supplies within the system shall be operating between 18.7A to 21.3A (+/- 6.5% of 20A).

All current sharing functions shall be implemented internal to the power supply by making use of the SBus signal. The power distribution board (Housing Back Plane, for example YH-Part), must connect the SBus signals between the power supplies together. The power supply shall be able to share with up to 1+N supply in parallel.

The failure of a power supply shall not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with 100mV of drop between different power supply's output.

If the load sharing is disabled by shorting the load share bus to ground, the power supply shall continue to operate within regulation limits for loads less than or equal to the rating of one power supply.

Table 18 - Load share bus output characteristics

Item	Description	Min	Nominal	Max	Units
V_{share}; I_{out}=Max.	Voltage of load share bus at specified max output current		8		V
$\triangle V_{share}/\triangle I_{out}$	Slope of load share bus voltage with changing load		8 /I_{outmax}		V/A
I_{share}SINK	Amount of current the load share bus output from each power supply is allowed to sink		1.5		mA
I_{share}SOURCE	Amount of current the load share bus output from each power supply needs to source		1.5		mA
T_{share}; I_{out}=Max.	Delay from output voltages in regulation to load sharing active with maximum load of one power supply and two power supplies in parallel. (remote on/off only)			100	msec

3.3 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For 5Vsb, it is allowed to rise from 1 to 25ms. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

3.3.1 Output Voltage Timing

The timing of signals and outputs are specified in below Table 19 and illustrated in Figure 2.

Table 19 - Turn on/off timing

Turn on	Description	Min	Max	Units
$T_{vout\ rise}$	Output voltage rise time for all main output	5*	70*	msec
$T_{sb\_on\_delay}$	Delay from AC being applied to 5Vsb being within regulation		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltage being within regulation		2500	msec
T_{vout_holdup}	Time all main output 12VI voltages stay within regulation after loss of AC.	12		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	11		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits	5	400	msec
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltage(12V) within regulation limits to PWOK asserted at turn on	100	500	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal	100		msec
T_{sb_vout}	Delay from 5Vsb being in regulation to main output being in regulation at AC turn on.	50	1000	msec
T_{5Vsb_holdup}	Time the 5Vsb output voltage stays within regulation after loss of AC	70		msec

*T_{vout_rise} :The 5Vsb and -12V output rise time shall be 1ms to 25ms.

Figure 2 – Output Voltage timing

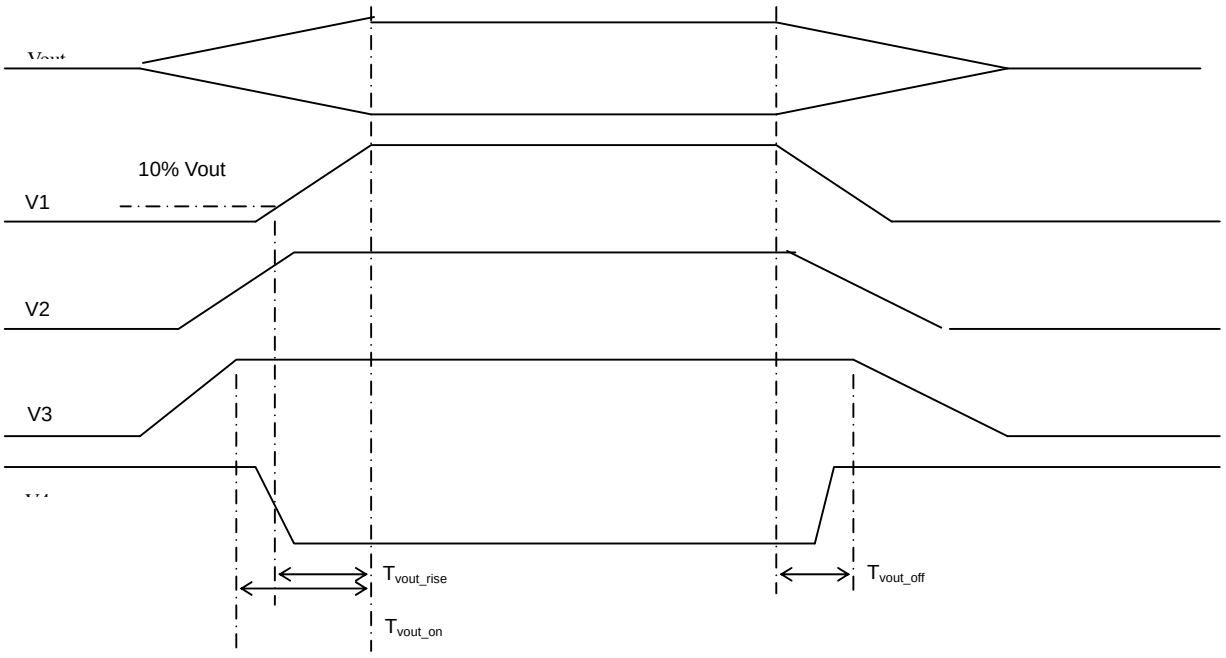
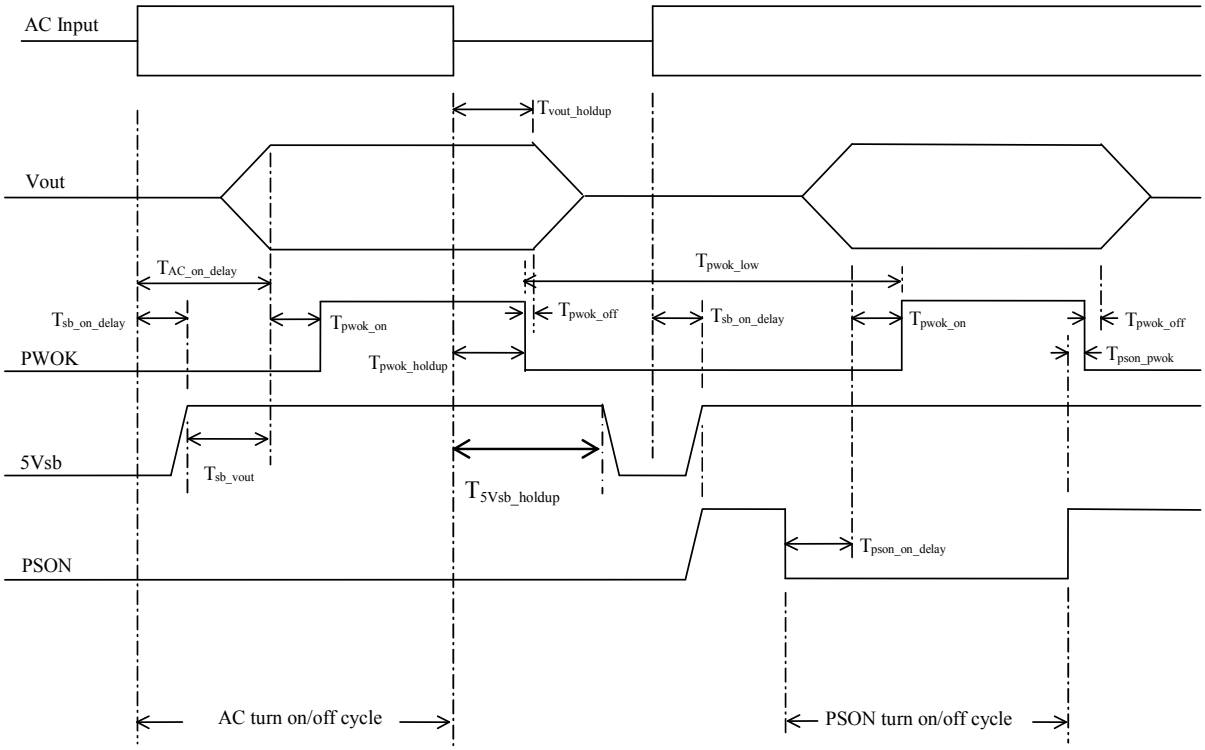


Figure 3 – Turn On/Off Timing (Power Supply Signals)



3.3.2 Overshoot

Any output overshoot at turn on shall be less than 10% of the nominal output value.

3.3.3 Undershoot

Any output shall not undershoot at turn on or off cycle under any circumstances.

3.4 Control and Indicator functions

The following section define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention:

Signal# = low true.

3.4.1 PSON# Input Signal (Power supply enable)

The PSON# signal is required to remotely turn on/off the main output of the power supply.

PSON# is and active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off.

PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply. See Table 20.

Table 20 – PS ON# signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to 5V located in the power supply.**	
PSON# = Low	ON	
PSON# = High or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, V_{pson} = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		50ms

3.4.2 Power OK (PG or PWOK) Output Signal

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, a internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit. See Table 21.

Table 21 – PWOK signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to 5V located in power supply.**	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{source} = 200μA	2.4V	5.25V
Sink current, PWOK=low		4mA
Source current, PWOK=high		2mA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100μsec
Power down delay: T_{pwok_off}	1ms	200ms

3.4.3 SMBAlert# (PSAlert) Output Signal Pin

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.
This signal is to be asserted in parallel with LED turning solid red or blinking red/blue. See Table 22.

Table 22 – SMBAlert# signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to 5V located in power supply.**	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{sink} = 50µA	2.4V	5.25V
Sink current, Alert#=low		4mA
Sink current, Alert#=high		2mA
Rise and fall time		100µsec

3.4.4 A0

PSU Module Address Line 0. This signal line is provided for determining the address for the specific PSU FRU and SMBus address. The pull-up resister should be located in the system and the pull-up voltage should be limited to 3.3V. The address line should be pull low with equal to or less than 100ohm in the motherboard design.

3.4.5 A1

PSU Module Address Line 1. This signal line is provided for determining the address for the specific PSU FRU and SMBus address. The pull-up resister should be located in the system and the pull-up voltage should be limited to 3.3V. The address line should be pull low with equal to or less than 100ohm in the motherboard design.

3.4.6 $12V_{RS}$ and Return Sense

The power supply has remote sense return (Return Sense) to regulate out ground drops for all output voltages. The power supply uses remote sense to regulate out drops in the system for the main outputs. The +12V output only uses remote sense with reference to the Return Sense signal. The remote sense input impedance to the power supply must be greater than 10Ω on the main outputs and is 10Ω on Return Sense. These are the values of the resistors connecting the remote senses to the output voltage internal to the power supply. Remote sense is able to regulate out a minimum of 300mV of drop on the +12V output. The remote sense return is able to regulate out drops of 300mV as well. The current in any remote sense line shall be less than 5mA to prevent voltage sensing errors. The power supply operates within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

3.4.7 Present

This signal is connected to the power supply's output ground.

3.4.8 SDA and SCL

One pin is the serial clock (SCL), and the other pin is used for serial data (SDA). The SCL and SDA signals are pulled up by system, both pins are bi-directional, open drain signals, and are used to form a serial bus

4 Protection circuits

Protection circuits inside the power supply shall cause only the main output to shutdown (latch off). If the power supply latches off due to a protection circuit assert, an Input Power cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

Specific protection circuits shall not latch, but auto recover when the latching reason had been cleared. This protection circuits will be written in cursive writing and will have a Auto Recover ($Output_{AR}$) in the chapter name.

The auxiliary output shall not affected by any protection circuit, unless the auxiliary output itself is affected.

4.1 Over Voltage Protection (OVP_{main} & $OVP_{auxiliary\ AR}$)

All Over Voltage Condition shall be measured internal to the power supply on all outputs (Main and Auxiliary $Output_{AR}$) at the card edge output. The power supply shall shutdown and latch off after an Over Voltage condition occurs on main outputs, the auxiliary output shall be auto recover **(VsB_{AR})** after the OVP had been removed.
The voltages never shall exceed the maximum levels specified in below table when measured during any fail.

The power supply shall alert the system of the OVP condition via SMBAlert# and fail LED indicator.
The latch on the main output can be cleared by asserting the PSON# signal or by an Input Power interruption.

Table 23 - Over Voltage Protection requirements

Output Voltage	MIN (V)	MAX (V)
+3.3 V	3.9	4.5
+5 V	5.7	6.5
+12 V	13.3	14.5
-12 V	-13.3	-14.5
+5Vsb	5.7	6.5

4.2 Over Current and Short Circuit Protection (OCP/SCP_{main} & $OCP/SCP_{auxiliary\ AR}$)

The Over Current Condition shall be measured internal to the power supply on all outputs (Main and Auxiliary $Output_{AR}$), and preventing outputs to exceed current limits specified in below table. The power supply shall shutdown and Auto Recover after an Over Current condition on main outputs, the auxiliary output shall be auto recover **(VsB_{AR})** after the OCP/SCP had been removed.

The latch on the main output can be cleared by asserting PSON# signal or by an Input Power interruption.
The power supply shall alert the system of the OCP/SCP condition via SMBAlert# and fail LED indicator.
The power supply shall not be damaged from repeated power cycling in this condition.

Table 24 – Over Current/Short Circuit Protection

Voltage	Over Current Limit (Iout limit)
+3.3 V	110% minimum; 150% maximum
+5 V	110% minimum; 150% maximum
+12 V	120% minimum; 150% maximum

4.3 Over Temperature Protection (OTP_{AR})

The power supply shall have minimum of two thermal sensors to measure the environmental (T_{env}) and critical component (T_{comp}) temperature. The thermal sensors shall be part of a protection circuit to protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an critical Over temperature condition, specified in below table, the PSU shall be shutdown with the exception of the **auxiliary output (VsB_{AR})**.

The power supply shall alert the system of the **OTP_{AR}** condition via SMBAlert# and fail LED indicator. The power supply will auto recover from this condition, when the temperature is dropping within specification again. If the **OTP_{AR}** is caused due to a defective fan, the power supply shall latch off and not auto recover.

Table 25 – Over Temperature Protection$_{AR}$

Condition	Warning in °C	Critical in°C	Timing for SMBAlert#/LED
T_{env}	70	75	1msec
T_{comp}	95	100	1msec

4.4. Fan Failure Protection$_{AR}$

The power supply shall have a circuit internal to monitor the power supply internal fan. The fan failure protection shall monitor the fan speed and should assert SMBAlert# and fail LED signal in case the fan Rotation Per Minute (RPM) drop lower threshold or set PWM Δ as defined in below table.

The protection circuit shall shutoff the main outputs only and let them auto recover when the fan failure had been cleared.

Table 26 – Fan Failure Protection$_{AR}$

Condition	FAN RPM	Timing for SMBAlert#/LED
Warning	1500	1sec
Critical	1000	1sec

5 Power Supply Management

5.1 Hardware Layer

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 “high power” and I^2C Vdd based power and drive specification.

This bus shall operate at 3.3V but be tolerant to 5V pull-ups. The power supply should not have any internal pull-ups on the SMBus, pull-ups shall be located on system side.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their 3.3V power from the 5Vsb bus through a buffer. Device(s) shall be powered from the system side of the 5Vsb oring device. No pull-up resistors shall be on SCL or SDA inside the power supply. The pull-up resistors should be located external to the power supply on system/application side.

5.2 Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the 5Vsb output on the system side of the oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2 or later

It shall be located at the address set by the A0 and A1 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

Table 27 – PSMC Addressing

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h
Pin A1/A0	0/0	0/1

5.2.1 Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.1 and 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.1 and 1.2
- System Management Bus (SMBUS) Specification 2.0

5.2.2 Data Speed

The PSMC device in the power supply shall operate at the full 100kbps (100kHz) SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply is allowed to clock stretch while parsing a command or servicing multiple interrupts or NACK.

Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

The PSMC may support 400kbps (400kHz) PMBus speed.

5.2.3 Bus Errors

The PSMC shall support SMBus clock-low timeout ($T_{timeout}$). This capability requires the PSMC to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions within 10ms later. The total reset time from detection of the condition till restarted, ready to receive commands condition shall not exceed 35ms.

The device must recognize SMBus START and STOP conditions on ANY clock interval. The PSMC must not hang due to ‘runt clocks’, ‘runt data’, or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup. Or hold times that are shorter than the minimums specified by the SMBus specifications. The PSMC is not required to operate normally, but must return to normal operation once ‘in spec’ clock and data timing is again received. Note if the PSMC ‘misses’ a clock from the master due to noise or other bus errors, the device must continue to accept ‘in spec’ clocks and NACK. The PSMC is suppose to re-synch with the master on the next START or STOP condition.

5.2.4 Write byte/word

The first byte of a Write Byte/Word access is the command code. The next one or two bytes, respectively, are the data to be written. In this example the master asserts the slave device address followed by the write bit. The device acknowledges and the master delivers the command code. The slave again acknowledges before the master sends the data byte or word (low byte first). The slave acknowledges each byte, and the entire transaction is finished with a STOP condition.

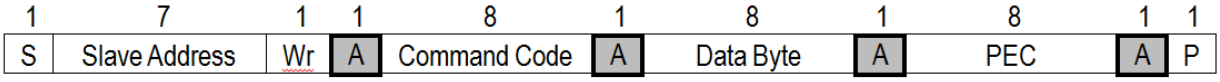


Figure 4 –Write byte protocol with PEC

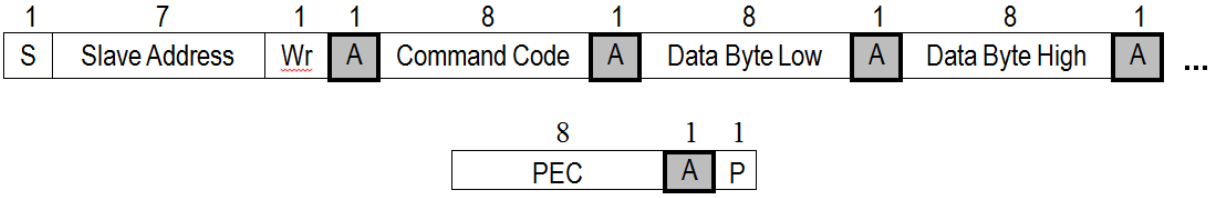


Figure 5 –Write Word Protocol with PEC

5.2.5 Read byte/word

Reading data is slightly more complicated than writing data. First the host must write a command to the slave device. Then it must follow that command with a repeated START condition to denote a read from that device's address. The slave then returns one or two bytes of data.

Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

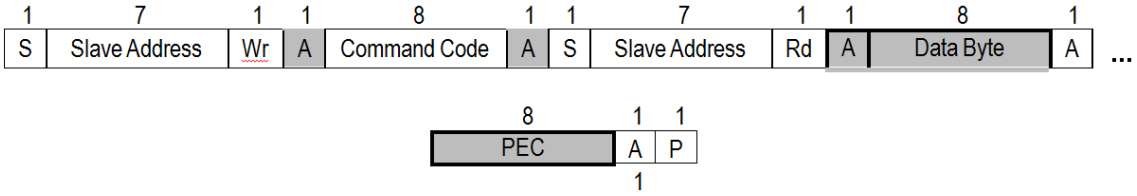


Figure 6 –Read byte protocol with PEC

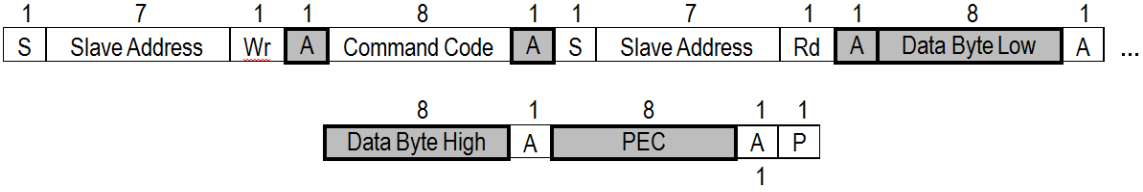


Figure 7 –Read word protocol with PEC

5.2.6 Block write/read

The Block Write begins with a slave address and a write condition. After the command code the host issues a byte count which describes how many more bytes will follow in the message. If a slave has 20 bytes to send, the byte count field will have the value 20 (14h), followed by the 20 bytes of data. The byte count does not include the PEC byte. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

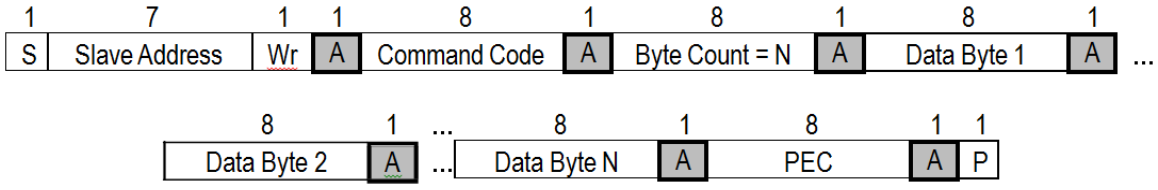


Figure 8 –Block Write with PEC

A Block Read differs from a block write in that the repeated START condition exists to satisfy the requirement for a change in the transfer direction. A NACK immediately preceding the STOP condition signifies the end of the read transfer.

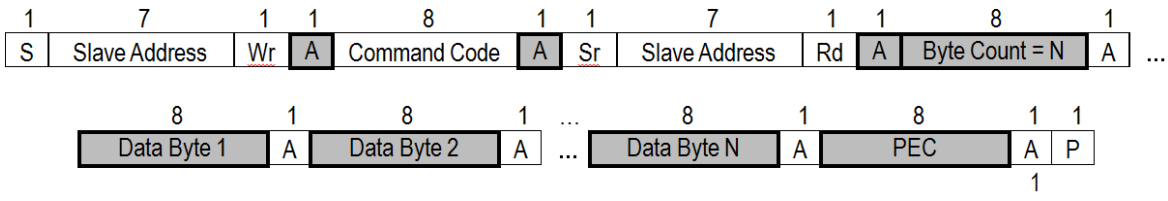


Figure 9 –Block Read with PEC

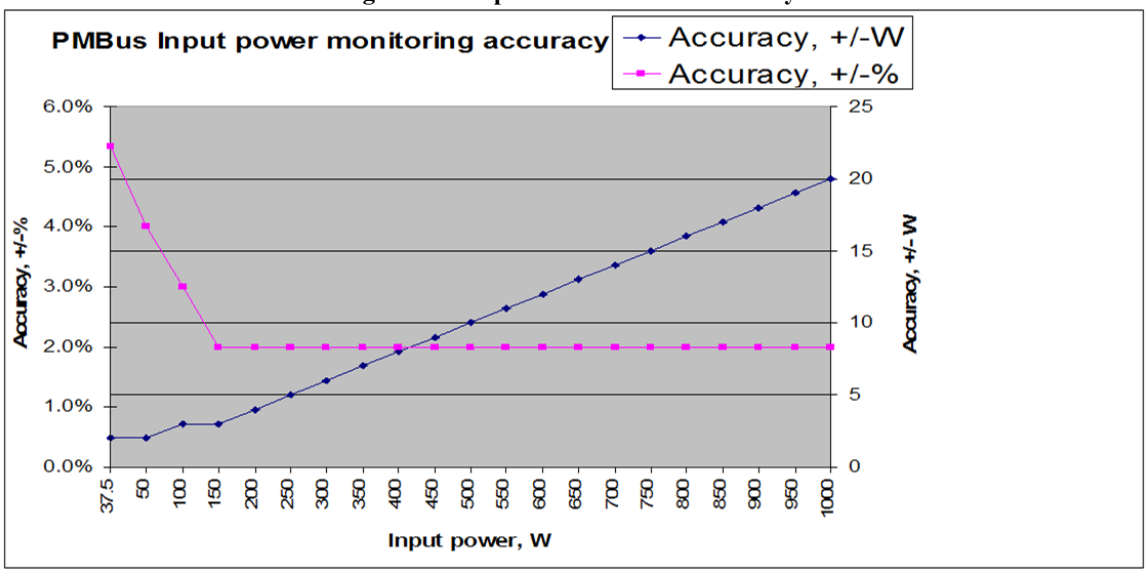
5.2.7 Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be meet at the specified environmental condition and the full range of rated input voltage.

Table 28 – Sensor Accuracy

Sensor	10% - 20% load	> 20% - 50% load	> 50% - 100% Load
Current	± 5%	± 2%	± 2%
FAN	± 10% from Spec.		
Input Power	± 5%	± 2%	± 2%
	See Figure 10		

Figure 10 – Input Power Sensor Accuracy



5.2.8 PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose.

All Sensors shall continue to provide real time data as long as the PSMC device is powered.

This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 29 – PSMC Sensor list

Sensor	Description
V_{input}	Input Voltage
I_{input}	Input Current
P_{input}	Input Power
V_{output_main}	Output Voltage main output
I_{output_main}	Output Current main output
P_{output_main}	Output Power main output
V_{output_aux}	Output Voltage auxiliary output
I_{output_aux}	Output Current auxiliary output
P_{output_aux}	Output Power auxiliary output
T_{comp}	Component Temperature
T_{env}	Environmental Temperature
RPM_{Fan}	Fan Speed reading

5.3 Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I^2C bus. Four pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0 . SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I^2C bus . A0 and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I^2C address shall be per table below.

The device used for this shall be powered from a 3.3V bias voltage derived from the 5Vsb output . No pull-up resistors shall be on SCL or SDA inside the power supply.

Table 30 - EEPROM Addressing

PDB position and FRU address	PM1 A0h/A1h	PM2 A2h/A3h
Pin A1/A0	0/0	0/1

5.3.1 FRU Data

The FRU Data format shall be compliant with the IPMI ver. 1.0 (per rev. 1.1 from Sep.25th , 1999) specification. The current version of these specification is available at http://developer.intel.com/design/servers/ipmi/specs.htm. The following is the exact listing of the EEPROM content. During testing this should be followed and verified.

5.3.2 FRU Device protocol

The FRU device will implement the same protocols as the commonly used the memory device, including Byte Read, Sequential Read, Byte Write, and Page Read protocols.

5.3.3. FRU Data Format

The information to be contained in the FRU device is shown in the following table.

Table 31 - EEPROM Addressing

Area Type	**Description**
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document. Product information shall be defined as follows:
Field Name	**Field Description**
Manufacturer Name	FSP Technology Inc.
Product Name	FSP1200-50DRS
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}
Multi-Record Area	As defined by the IPMI FRU document. The following record types shall be used on this power supply: - Power Supply Information (Record Type 0x00) - DC Output (Record Type 0x01) No other record types are required for the power supply. Multi-Record information shall be defined as follows:
Field Name (PS Info)	**Field Information Definition**
Overall Capacity (watts)	900W for 90~140Vrms 1200W for180~264Vrms
Peak VA	
Inrush current (A)	80
Inrush interval (msec)	5
Low end input voltage range 1	90
High end input voltage range 1	140
Low end input voltage range 2	180
High end input voltage range 2	264
A/C dropout total. (msec)	12
Binary flags	Set for: Hot Swap support, Auto switch, and PFC
Peak Wattage	Set for: 1200Watts
Combined wattage	None
Predictive fail tach support	Supported
Field Name (Output)	Field Description:
Output Information	Set for: Standby on +5Vsb, No Standby on all others.
All other output fields	Format per IPMI specification, using parameters in this specification.

5.3.4 FRU Signals

Four pins will be allocated for the FRU information on the Power Supply connector. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

Table 32 - FRU Signals

A1	A0	MCU	PSU
0	0	B0	1
0	1	B2	2
1	0	B4	3
1	1	B6	4

6. Smart On Function

6.1 PMBus command for Smart On

6.1.1 Hardware Connection

Before enabling Smart On function, make sure pin B22 (SMART ON) on output golden finger of each PSU is connected together.

6.1.2 Configuring Smart On with SMART_ON_CONFIG (D0h)

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to Smart On. We will call the command SMART_ON_CONFIG (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

Table 33 - SMART_ON_CONFIG (D0h)

Value	State	Description
00h	Standard Redundancy	Turns the power supply ON into standard redundant load sharing mode.
01h	Smart On Active	Defines this power supply to be the one that is always ON in a Smart On configuration.
02h	Smart Standby	Defines the power supply that to turn off in a Smart On configuration and first to turn on as the load increases.

The default state of power supply is in Standard Redundancy mode. Power supply need to be re-specified a state whenever initial power on or any power supply in the system is in fault situation.
The SMART_ON_CONFIG command will reset to 00h (Standard Redundancy) when any fault or over current happened. The faults include AC loss, over hot spot temperature, over ambient temperature, +12V short internally (under voltage), +12V over voltage, fan locked, D2D controller soft-start short.

6.2 Smart Standby Power Supply Operating State

A power supply is put into Smart Standby whenever PSON# is asserted, and SMART_ON_CONFIG value is set to 02h. In the Smart Standby mode the power supply must:

1. Power ON when Smart_On bus is driven LOW
2. Keep PWOK asserted
3. No PMBus fault or warning conditions reported via STATUS commands
4. keep all fans rolling
5. LED is blue blinking

6.2.1 Powering on Smart Standby supplies to maintain best efficiency

Power supplies in Smart Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position the system defines that power supply to be in the Smart Standby configuration; will slightly change the load share threshold that the power supply shall power on at.

6.2.2 Powering on Smart Standby supplies during a fault or over current condition

Some warnings happen or 12V output shutdown due to any fault. When an active power supply asserts, all parallel power supplies in Smart Standby mode shall power on immediately.

The trigger condition:

1. 12V OC warning/ fault happens

2. 12V OVP fault

3. 12V UVP

4. OTP warning/ fault

5. fan speed warning/ fault

6.AC loss(low than 75V +/-5V)

When an active power supply asserts, all parallel power supplies in Smart Standby mode shall power on immediately.

6.3 The Way to Enable Smart On Function

Here are the steps to put PSU into smart on mode. PSU which is assigned as smart on standby can operate in a power-off state and turn on main power if necessary.

The trigger levels above may have a +/-10% tolerance for actual application.

Step1: Make sure every PSU has AC power cord applied. Use write byte command to set command 0xD0 for each PSU to has it own role (must one PSU as active role).

The command format for Smart On function will be as following example.

B0 in smart_on_active (S B0 w D0 01 PEC P)

B2 in smart_on_standby (S B2 w D0 02 PEC P)

Step2: PSU will enter smart slave mode once the load is lower than the corresponding trigger point.

Step3: If SMART_ON (pin B22) signal falls to low, all PSU will turn on the main power and reset smart_config to 0x00 (standard redundancy). System needs to re-assign the roles for all PSU to enable smart on function again.

7 ENVIRONMENTAL

The power supply shall operate normally, and sustain no damage as a result of the environmental conditions listed in this chapter.

7.1 Temperature

Operating Ambient, normal mode (inlet Air): 0°C min/+50°C max at 5000m above sea level.
(At full load, with a maximum rate of change of 5°C/10 minutes, but no more than 10°C/hr)
Operating Ambient, stand-by mode (inlet Air): -5°C min/+50°C max at 5000m above sea level.
Non-operating ambient: -40°C to +70°C (Maximum rate of change shall be 20°C/hr)

7.2 Humidity

Operating: up to 85% relative humidity (non-condensing)
Non-operating: up to 95% relative humidity (non-condensing)
Note: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

7.3 Altitude

A) Operation : sea level to 5,000m
B) Non-Operation : sea level to 15,200m

7.4 Vibration

A) Operation : 0.01g²/Hz at 5 Hz sloping to 0.02g²/Hz at 20 Hz, and maintaining 0.02g²/Hz from 20 Hz to 500 Hz. The area under the PSD curve is 3.13gRMS. The duration shall be 20 minutes per axis for all three axes on all samples.
B) Non-Operation :

- **Sine sweep:** 5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15min at each of 3 resonant points;

7.5 Mechanical Shock

A) Operation: 10G, no malfunction
B) Non-operating: 50G Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

7.6 Thermal shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30minutes.

7.7 Catastrophic Failure

The power supply shall be designed to fail without startling noise or excessive smoke.

7.8 EMI

The power supply shall comply with FCC part 15, CRISP 22 and EN55-22; Class A for both conducted and radiated emissions with a 3dB margin. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Test will be performed at 115VAC@60Hz and 230VAC @ 50Hz power.

The power supply shall comply with EN55024.

The power supply when installed in the system must meet the following all the immunity requirements when integrated into the end system.

7.9 Magnetic Leakage Fields

The PFC choke magnetic leakage field shall not cause any interference with a high resolution computer monitor placed next to or on top of the chassis.

7.10 Voltage Fluctuations and Flicker

The power supply shall meet the specified limits of EN61000-3-3, for voltage fluctuations and flicker for equipment ≤ 16 amps connected to low voltage distribution systems.

8 REGULATORY Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.) other than ITE application, may require further evaluation.

8.1 Product Safety Compliance

A) UL 60950-1/CSA 60950-1 Edition 2 (USA/Canada)
B) EN60950-1 Edition 2 (Europe)
C) IEC60950-1 Edition 2 (International)
D) CB Certificate & Report, IEC60950-1 Edition 2 (report to include all country national deviations)
E) CE – Low Voltage Directive 2006/95/EC (Europe)
F) BSMI (Taiwan)
G) GB4943-CBCA Certification (China)

8.2 Product EMC Compliance – Class A Compliance

Note: The product is required to comply with Class A emission, as the system it is build into might be configured with the intend for commercial environment or home use. The Power supply is to have a minimum of 3dB margin to Class A Limits to support FSP's Standard margin requirements.

A) FCC / ICES-003 Emission (USA/Canada) Verification
B) CRISP 22 – Emission (International)
C) EN55022 – Emission (Europe)
D) EN55024 – Immunity (Europe)
   - EN61000-4-2 Electrostatic Discharge
   - EN61000-4-3 Radiated RFI Immunity
   - EN61000-4-4 Electrical Fast Transients
   - EN61000-4-5 Electrical Surge
   - EN61000-4-6 RF Conducted
   - EN61000-4-8 Power Frequency Magnetic Fields
   - EN61000-4-11 Voltage Dips and Interruptions
E) EN61000-3-2 – Harmonics (Europe)
F) EN61000-3-3 – Voltage Flicker (Europe)
G) CE – EMC Directive 2004/108/EEC (Europe)
H) JEIDA (Japan)
I) AS/NZS CISPR 22 (Australia / New Zealand)
J) BSMI (Taiwan)
K) GB 9254 2008 (EMC) Certification (China)
L) GB 17625.1 – (Harmonics) CNCA Certification (China)

8.3 Maximum AC Leakage current to ground

3.5mA max for each power supply at 240Vac.

8.3.1 Hi-pot

The power supply module in the system shall be test at 1800Vac, with a trigger limit of 30mA.

8.4 Electrostatic Discharge (ESD)

In addition to IEC 801-2/ IEC1000-4-2, the following ESD tests shall be conducted. Each surface area of the system under test shall be subjected to twenty (20) successive static discharges, at each of the following voltages: 2kV , 3kV , 4kV , 5kV , 6kV , 7kV , 8kV , 10kV , 15kV.

Performance criteria:

a) All power system output shall continue to operate within the limits of this specification, without glitches or interruption, while the supply is operated as defined and subjected to 2kV through 15kV ESD pulses. The direct ESD event shall not cause any out of regulation condition. The power system shall withstand these tests without nuisance trips.

b) The power system, while operating as defined, shall not have a component failure when subjected to any discharge voltages up to and including 15kV. Component failure is defined as any malfunction of the power supply caused by component degradation or failure requiring component replacement to correct the problem.

8.5 Certifications / Registrations/ Declarations

A) UL Certification (US)
B) CB Certification & Report
C) TÜV Rheinland (Germany)
D) CE Declaration of Conformity (CENELEC Europe)
E) BSMI (Taiwan)
F) CCC / CNCA Certification (China)

8.6 Component Regulation Requirements

1. All Fans shall have the minimum certifications: UL and TÜV or VDE
2. All current limiting devices shall have UL and TÜV or VDE certifications and shall be suitable rated for the application where the device In its application complies with IEC60950.
3. All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printing wiring board manufacturer.
4. All connectors shall be UL recognized and have a UL flame rating of UL94V-0
5. All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer.
   SELV cable to be rated minimum 80V @ 120°C
6. Product safety label must be printed on UL approved label stock and printer ribbon.
   Alternatively labels can be purchased from a UL approved label manufacturer.
7. The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

8.6.1 Product Ecology Requirement

All materials, parts and subassemblies must not contain restricted materials as defined in directive 2002/95/EC, Restriction of Hazardous Substances (RoHS) 6/6.

All cords and cables shall contain <100ppm of cadmium.

All packing materials must be marked with applicable recycling logos for Europe (green dot) and Japan (Eco-marks), if sold as a retail product. All packing materials shall be recyclable.

9 Reliability / Warranty / Service

9.1 Mean Time between Failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25°C excluding the Fan MTBF, and at least 100,000 hours including the fan MTBF.

9.2 Warranty

The Warranty for the power supply is 36 months (three years) from production date code.

9.3 Serviceability

No troubleshooting by maintenance personnel is to be performed. Units shall be returned to FSP Power for any troubleshooting, unless agreed by both parties.

The power supply will lose warranty if opened other than FSP service personal or agreed by both parties.

10 MISCELLANEOUS

10.1 Marking

The Power Supply shall carry labels defined in this section.

10.2 Outline Dimensions

The Power Supply module shall have the dimension 38.5mm x 73mm x265mm (HxWxL) without the card edge.

10.2.1 Power Supply Card Edge Dimension

The Power Supply Card Edge shall comply with below specification.

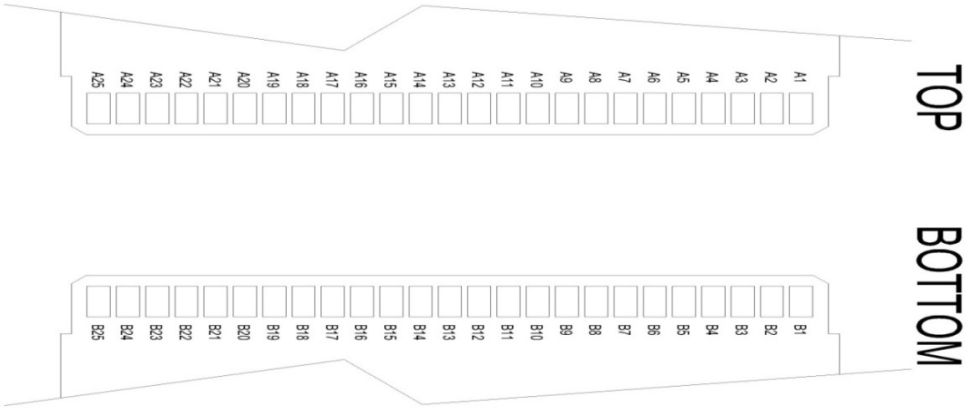


Figure 11 – Card Edge Dimension

Pin Name	Signal Name	Function
A1 ~ A9	GND	+12V return
B1 ~ B9	GND	+12V return
A10 ~ A18	Main Output	+12V
B10 ~ B18	Main Output	+12V
A19	SDA	I^2C Data signal
A20	SCL	I^2C Clock signal
A21	PSON	Power enable input
A22	SMB_Alert	SMB_Alert for failure notification
A23	Return Sense	+12V RTN Sense
A24	+12V Remote Sense	+12VS
A25	PWOK	Power OK output
B19	A0	I^2C address bit 0
B20	A1	I^2C address bit 1
B21	Standby_Output	+5Vsb
B22	Smart ON	Smart ON
B23	SBus	+12V Main output Current share bus
B24	PRESENT	GND
B25	AC Fail	AC Fail Warning signal

10.3 Packing

The Power Supply should be packed according to the description in this chapter.
The Packing for the power supply should be recyclable and has no metal parts to hold the packing.

11 PSMC Interface

Following chapter provide details information of the utilized PSMC interface protocol utilized. The Interface protocol can be recognized by it's ID.

By Default the PMBus shall be utilized to achieve the best compatibility with current applications.

A customization of the PSMC Interface is possible and would accordingly reflected in a different FW ID and different specification compared to the PMBus ones.

11.1 PMBus Data Format

The Linear Data Format is a two byte value with:

An 11 bit, two's complement mantissa and

A 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure 12.

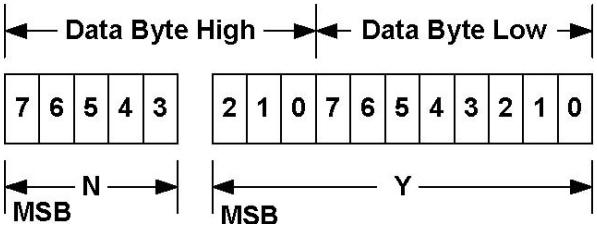


Figure 12. Linear Data Format Data Bytes

The relation between Y, N and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value being communicated

Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of N.

11.2 Power Sensors

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the power supply shall be zero amps and zero volts.

Table 34 – PMBus Command Summary supported

Command Code	Name	Type	Bytes	Conditions
00h	PAGE	R/W Byte	1	
01h	OPERATION	R/W Byte		
02h	ON_OFF_CONFIG	R/W Byte		
03h	CLEAR_FAULTS	Send Byte	0	
05h	PAGE_PLUS_WRITE	Block Write		
06h	PAGE_PLUS_READ	Block Write – Block Read Process Call		
19h	CAPABILITY	Read Byte	1	Value by capability
1Ah	QUERY	Block Write-Block Read Process Call	See PMBUS SPEC	
1Bh	SMBALERT_MASK	Write Word	2	
20h	VOUT_MODE	Read Byte	1	
3Ah	FAN_CONFIG_1_2	**Read Byte**	1	
3Bh	FAN_COMMAND_1	R/W Word	2	
4Ah	IOUT_OC_WARN_LIMIT	**Read Word**	2	Page member
79h	STATUS_WORD	Read Word	2	
7Ah	STATUS_VOUT	Read Byte	1	
7Bh	STATUS_IOUT	Read Byte	1	Page member
7Ch	STATUS_INPUT	Read Byte	1	
7Dh	STATUS_TEMPERATURE	Read Byte	1	
81h	STATUS_FANS_1_2	Read Byte	1	
86h	READ_EIN	Block Read		
87h	READ_EOUT	Block Read		
88h	READ_VIN	Read Word	2	
89h	READ_IIN	Read Word	2	
8Bh	READ_VOUT	Read Word	2	Page member
8Ch	READ_IOUT	Read Word	2	Page member
8Dh	READ_TEMPERATURE_1	Read Word	2	
8Eh	READ_TEMPERATURE_2	Read Word	2	
90h	READ_FAN_SPEED_1	Read Word	2	
96h	READ_POUT	Read Word	2	
97h	READ_PIN	Read Word	2	
98h	PMBUS_REVISION	Read Byte	1	Value 22h
99h	MFR_ID	Read Block	Variable	FSP-GROUP
D0h	SMART_ON	R/W Word	2/1	
D1h	MFR_FW_ID	Read Block	Variable	Ex:1M.XXXX.XXXX.XXX
D4h	MFR_FW_DATE	Read Block	Variable	EX:13083001
D5h	MFR_FAN_DUTY	Read Byte		
D7h	MFR_CAL_INPUT	Block Write – Block Read		
D9h	MFR_EEPROM_WRITE	Block Write		
F8	BOOTLOADER COMMAND	Block Write		For boot loader
F9	BOOTLOADER OPERTAION	Write Byte		For boot loader
FA	BOOTLOADER CHECK SUM	Read Byte		For boot loader

11.2.1 PAGE Command (00h)

Page member :
READ_IOUT
READ_VOUT
STATUS_IOUT
STATUS_VOUT
IOUT_OC_WARN_LIMIT

Page list

PAGE	OUTPUT	Description
00h	12v1	Supported, Default for single 12v output
01h	12v2	--
02h	12v3	--
03h	12v4	--
04h	12v5	--
05h	12v6	--
06h-0fh	Reserved	--
10h	5v	Supported.
11h	3.3v	Supported.
12h-1fh	Reserved	--
20h	5vsb	Supported.
21h	3.3vsb	--
22h	-12v	Supported.
23h	12vsb	--
24h-2fh	Reserved	--
30h	48v	--
31h	24v	--
32h-3fh	Reserved	--

Note: " -- " is Not supported

11.2.2 Operation Command (01h)

Operation Notice：

This function is only supported for module operation only without PDB.

If utilized while inserted in a PDB without function support, utilization of this function might cause Unexpected side effects.

Operation command Default Value is 0x80h.

Bits [7:6]	Bits [5:4]	Bits [3:2]	Bits [1:0]	Unit On Or Off	Margin State	Description	Supported
00	XX	XX	XX	Immediate Off (No Sequencing)	N/A	Immediate turn-off	Ok
01	XX	XX	XX	Soft Off (With Sequencing)	N/A	turn-off delay and fall time	-
10	00	XX	XX	On (turn-on)	Off	Immediate turn-on	Ok
10	01	01	XX	On	Margin Low (Ignore Fault)	Margin Low (Ignore Fault)	-
10	01	10	XX	On	Margin Low (Act On Fault)	Margin Low (Act On Fault)	-
10	10	01	XX	On	Margin High (Ignore Fault)	Margin High (Ignore Fault)	-
10	10	10	XX	On	Margin High (Act On Fault)	Margin High (Act On Fault)	-

Note: " -- " is Not supported

11.2.3 ON_OFF_CONFIG Command (02h)

Operation Notice：

This function is only supported for module operation only without PDB.

If utilized while inserted in a PDB without function support, utilization of this function might cause Unexpected side effects.

ONOFF_CONFIG command Default value is 0x15h.

Bit	Purpose	Bit Value	Meaning	Default value	Supported
7:5	Reserved	Reserved	Reserved	Reserved	Reserved
4	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin	1	Ok
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).		
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus	0	Ok
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.		
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)	1	Ok
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.		
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)	0	-
		1	Active high (Pull high to start the unit)		
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay (Section 16.5) and fall time (Section 16.6)	1	-
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.		

Note: " -- " is Not supported

11.2.3.1 ON_OFF_CONFIG command operation note

Setting type	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Data value	Description[1]	Supported
1	0	X	X	X	0	0x00	If AC ok, turn-on power + DLY	-
2	0	X	X	X	1	0x01	If AC ok, turn-on power	OK
3	1	0	0	X	X	0x10	null	-
4	1	0	1	0	0	0x14	HW + LO + DLY	-
5	1	0	1	0	1	0x15	HW + LO	OK
6	1	0	1	1	0	0x16	HW + HI + DLY	-
7	1	0	1	1	1	0x17	HW + HI	-
8	1	1	0	X	0	0x18	SW + DLY	-
9	1	1	0	X	1	0x19	SW	OK
10	1	1	1	0	0	0x1C	HW + LO + SW + DLY	-
11	1	1	1	0	1	0x1D	HW + LO + SW	OK
12	1	1	1	1	0	0x1E	HW + HI + SW + DLY	-
13	1	1	1	1	1	0x1F	HW + HI + SW	-

Note: " -- " is Not supported

[1] :

X = don't care

HW = turn-on/off by control pin

HI = control pin active high turn-on power

LO = control pin active low turn-on power

SW = turn-on/off by operation command

DLY = turn-off delay

11.2.4 CLEAR_FAULTS Command (03h)

Operation Notice：

Null.

Power clear faults methods

The Power have four methods can be clear PMBus faults.

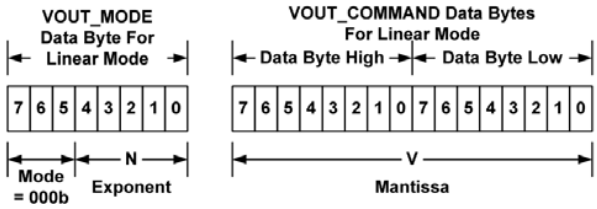
Method	Description
1	PMBus clear faults command
2	PMBus operation RESET[1]
3	PS RESET[1]
4	AC RESET[1]

[1] : RESET mean is Turn-OFF → Turn-ON

11.2.5 VOUT_MODE Command (20h)

The data bytes for the VOUT_MODE and VOUT_COMMAND when using the Linear voltage data format are shown in Figure .

Note that the VOUT_MODE command is sent separately from output voltage related commands and only when the output voltage format changes. VOUT_MODE is not sent every time an output voltage command is sent.



The Mode bits are set to 000b.

The Voltage, in volts, is calculated from the equation:

Voltage = $V \cdot 2^N$

Where:

Voltage is the parameter of interest in volts;

V is a 16 bit unsigned binary integer; and

N is a 5 bit two's complement binary integer.

11.2.6 STATUS_WORD Command (79h)

Byte	Bit Number	Status Bit Name	Meaning	Supported
Low	7	BUSY	A fault was declared because the device was busy and unable to respond.	-
	6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	Ok
	5	VOUT_OV	An output overvoltage fault has occurred	Ok
	4	IOUT_OC	An output overcurrent fault has occurred	Ok
	3	VIN_UV	An input under voltage fault has occurred	Ok
	2	TEMPERATURE	A temperature fault or warning has occurred	Ok
	1	CML	A communications, memory or logic fault has occurred	-
	0	NONE OF THE ABOVE	A fault or warning not listed in bits [7:1] of this byte has occurred	-
High	7	VOUT	An output voltage fault or warning has occurred	Ok
	6	IOUT/POUT	An output current or output power fault or warning has occurred	Ok
	5	INPUT	An input voltage, input current, or input power fault or warning has occurred	Ok
	4	MFR	A manufacturer specific fault or warning has occurred	-
	3	POWER_ GOOD#	The POWER_GOOD signal, if present, is negated	Ok
	2	FANS	A fan or airflow fault or warning has occurred	Ok
	1	OTHER	A bit in STATUS_OTHER is set	-
	0	UNKNOWN	A fault type not given in bits [15:1] of the SATUS_WORD has been detected	-

Note: " -- " is Not supported

11.2.7 STATUS_VOUT Command (7Ah)

Bit	Meaning	Supported
7	VOUT Over voltage Fault	Ok
6	VOUT Over voltage Warning	Ok
5	VOUT Under voltage Warning	Ok
4	VOUT Under voltage Fault	Ok
3	VOUT_MAX Warning (An attempt has been made to set the output voltage to value higher than allowed by the VOUT_MAX command	-
2	TON_MAX_FAULT	-
1	TOFF_MAX Warning	-
0	VOUT Tracking Error	-

Note: " -- " is Not supported

11.2.8 STATUS_IOUT Command (7Bh)

Bit	Meaning	Supported
7	IOUT Over current Fault	Ok
6	IOUT Over current And Low Voltage Shutdown Fault	-
5	IOUT Over current Warning	Ok
4	IOUT Under current Fault	-
3	Current Share Fault	-
2	Power Limiting	-
1	POUT Over power Fault	-
0	POUT Over power Warning	-

Note: " -- " is Not supported

11.2.9 STATUS_INPUT Command (7Ch) (Module)

Bit	Meaning	Supported
7	VIN Over voltage Fault	-
6	VIN Over voltage Warning	-
5	VIN Under voltage Warning	Ok
4	VIN Under voltage Fault	Ok
3	Unit Is Off For Insufficient Input Voltage	Ok
2	IIN Over current Fault	-
1	IIN Over current Warning	-
0	PIN Over power Warning	-

Note: " -- " is Not supported

11.2.10 STATUS_TEMPERATURE Command (7Dh) (Module)

Bit	Meaning	Supported
7	Over temperature Fault	Ok
6	Over temperature Warning	Ok
5	Under temperature Warning	-
4	Under temperature Fault	-
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

Note: " -- " is Not supported

11.2.11 STATUS_FAN_1_2 Command (81h) (Module)

Bit	Meaning	Supported
7	Fan 1 Fault	Ok
6	Fan 2 Fault	Ok
5	Fan 1 Warning	Ok
4	Fan 2 Warning	Ok
3	Fan 1 Speed Overridden	Ok
2	Fan 2 Speed Overridden	-
1	Airflow Fault	-
0	Airflow Warning	-

Note: " -- " is Not supported

11.3 Firmware control rules(Module)

11.3.1 Auto fan control rule

1. Temperature and load control Fan duty cycle

   Fan duty =10 + [(140- ac voltage) * 0.5]+ [(Temperature - 25) * 0.5] + [(Iout - 20) * 1]

11.3.2 LED control rules(Module)

Event	Blue led	Red led
No AC power plug in.	OFF	OFF
AC ok + power turn-off.	Every 0.5sec blink once.	OFF
AC ok + power turn-on, no failure event.	ON	OFF
AC ok + power turn-on, failure event.	OFF	ON
AC ok + power turn-on, warning event.	Blue and Red led on every 0.5sec exchange of blink.	Blue and Red led on every 0.5sec exchange of blink.

11.4 Firmware Protection

1. Vout Over Voltage

Output voltage	Warn threshold	Protect threshold
12V	13V	13.9V
5V	5.5V	6.1V
3.3V	3.6V	4.2V
-12V	-13V	-13.3V
5VSB	5.5V	6.1V

2. Vout Under Voltage

Output voltage	Warn threshold	Protect threshold
12V	10V	9V
5V	4V	3.5V
3.3V	2.5V	2.65V
-12V	-10V	-9V
5VSB	4V	3.5V

3. Iout Over Current

Output voltage	Warning threshold	Protect threshold
12V	105A	120A
5V	32A	35A
3.3V	32A	35A
5VSB	6A	7A

4. Over Temperature(Module)

Temperature1：Power heat sink temperature
Temperature2：Environmental temperature

	Warning threshold	Protect threshold
Temperature 1	95℃	100℃
Temperature 2	70℃	75℃

5. Over Temperature Re-start(Module)

	Re-start temperature
Temperature 1	70℃
Temperature 2	60℃

6. AC Input Under Voltage(Module)

	Vin UV Protect threshold(hold 4sec)
AC Vin	80V
DC Vin	175V

7. Fan Speed Under Protection(Module)

	Warning threshold	Protect threshold
Fan 1	1500rpm	1000rpm

11.5 SMART_ON Command(D0h) (Module)

Value	State	Description
00h	Redundancy Mode	Turns the power supply ON into standard redundant load sharing mode.
01h	Active Mode	Defines this power supply is always ON in SMART ON configuration.
02h	Standby Mode	Defines the power supply that to turn off in a Smart On configuration and to turn on as the load increases.

11.6 Bootloader Funcion(F8h, F9h, FAh)

Command	Operation	Function
F8h	00	Enter boot mode
	01	Enter user mode
F9h	00	Write hex data
	01	Erase hex data
FAh		Read hex data checksum

Bootloader Flow:

STEP 1	0xB0 0xF8 0x01	Boot mode command
STEP 2	0xB0 0xF9 0x01	Erase RAM command
STEP 3	Wait 2000ms	Erase Time
STEP 4 STEP 5 STEP 6 Replay 4~6 STEP	0xB0 0xF9 0x00 Wait 1ms 32 bytes data	Write command Wait 1ms Write Data
STEP 7	Consecutive 32 data is 0xFF	Write to finish
STEP 8	Wait 140ms	Wait 140ms
STEP 9	0xB0 0xF8 0x00	Go to User mode
STEP 10	0xB0 0x00 0x00	Go to User mode
STEP 12	Wait 2000ms	Go to User mode Time
STEP 13	Read 0xB0 0xFA	Verify Checksum
		Finish

Hex File

An Intel HEX file is composed of any number of HEX records. Each record is made up of five fields that are arranged in the following format:

```
LLAAAATTDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDCC
10246200464C5549442050524F46494C4500464C33
||||||||||                                CC->Checksum
||||||||DD->Data
|||||||TT->Record Type
|||AAAA->Address
|LL->Record Length
```

Each group of letters corresponds to a different field. Each field is composed of at least two hexadecimal digits-which make up a byte-as described below:

File: Description:

LL This is the record-length field that represents the number of data bytes (dd) in the record.

AAAA This is the address field that represents the starting address for subsequent data in the record.

TT This is a field that represents the HEX record type, which may be one of the following:

00 - data record

01 - end-of-file record

02 - extended segment address record

04 - extended linear address record

DD This is a data field that represents one byte of data. A record may have multiple data bytes. The number of data bytes in the record must match the number specified by the ll field.

CC This is the checksum field that represents the checksum of the record. The checksum is calculated by summing the values of all hexadecimal digit pairs in the record modulo 256 and taking the two's complement.