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SPECIFICATION



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YH5651-1TA02R

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1. GENERAL

This specification describes the performance characteristic of a up to 650W hot swappable, N+1 power system, The system is configured to hold up to two identical 650W (YM-2651TA01R) power supply module with +12V, +5Vsb output. The main DC outputs for the YH5651-1TA02R are +3.3V, +5V, +12V, -12V main DC outputs and a +5VSB standby output.

2. ELECTRICAL PERFORMANCE

2.1. AC Power Input

2.1.1. Input Voltage and Frequency

The power supply shall be capable of supplying full rated output power in the voltage range of 90Vac to 264Vac from a single phase source. The power supply shall operate at any input frequency between 47Hz to 63Hz. The nominal voltage is 115Vac for a voltage source with 90-132V range, and is 230Vac for a voltage source with 180 to 264V range.

Table 1 – Rated output power for each input voltage range

	Min	Nominal	Max
Nominal Range1	90VAC	115VAC	132VAC
Nominal Range2	180VAC	230VAC	264VAC

2.1.2. Input Current

The maximum input current for each input voltage range of Table 2

Table 2 – Maximum input current

Input voltage	Maximum input current
	650W
90-132V	10A
180-264V	5A

2.1.3. AC Line Inrush

The maximum ac line inrush current shall be 55A peak at an input voltage of 264Vac. 1+1 redundant maximum AC line inrush current shall be 100A peak at an input voltage of 264Vac. Inrush current shall be measured at an ambient temperature of 25 deg C after the input voltage has been removed from the power supply for a minimum of 10 minutes.

2.1.4. Input Power Factor

The input power factor shall be greater than 0.95 at nominal input voltages at the power supply's rated outputs. The power factor shall be greater than 0.90 at nominal input voltages at 50% rated outputs.

2.1.5. AC Line Dropout

An AC line dropout is a transient condition defined as the AC input to the power supply drops to 0 Vrms for 16ms. An AC line dropout shall not damage the power supply under any load condition. During an AC line dropout, the power supply must meet voltage regulation requirements in section 2.3 over the rated load. An AC line dropout shall not cause any power supply protection circuit to trip.

If the AC line dropout transient lasts longer than one input frequency period, the power supply may shutdown or go out of regulation. A dropout period of any length shall not cause damage to the power supply.



2.1.6. Efficiency

80% minimum at 115Vac/230Vac for the rated load specified in Table 6.

2.2. Control and Indicator Functions

Signals that can be defined as low true or high true shall adopt the following convention:
signal[#] = low true.

2.2.1. PSON[#] (Power supply enable)

The PSON[#] signal is required to remotely turn on/off the 12 VDC output in the power supply. When the power supply is in standby mode the power supply fan shall be OFF. PSON[#] is pulled to a standby voltage by a pull-up resistor internal to the power supply. See Table 3.

Table 3 – PS ON[#] signal characteristics

Signal Type	Pull-up to +5VCC located power supply	
PSON [#] = Low, PSKILL = Low	ON	
PSON [#] = Open, PSKILL = Low or Open	OFF	
PSON [#] = Low, PSKILL = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, Vpson = low		1mA

2.2.2. PWOK (Power Good Signal)

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are above their respective lower regulation limits. See Table 4.

Table 4 – PWOK signal characteristics

Signal Type	Pull-up to +5VCC located power supply	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isource = 200uA	2.4V	5.25V
Sink current, PWOK=low		4mA
Source current, PWOK=high		2mA

2.2.3. TTL Signal

A TTL compatible, active high signal shall become active. Two such signals shall be provided, each corresponding to one of the 1+1 modules. Each is capable to sink 5mA and source 400uA.



Signal Type	Pull-up to +5VCC located power supply	
TTL signal=high	Power Good	
TTL signal=low	Power Not Good	
	MIN	MAX
Logic level low voltage, Isink=5mA	0V	0.4V
Logic level high voltage, Isource = 400uA	2.4V	5.25V

2.2.4. ALARM MUTE Signal

An audible alarm shall sound. This alarm can be turned off by an active low TTL compatible open collector signal applied to alarm reset *MUTE.

Signal Type	Pull-up to +5VCC located power supply	
ALARM MUTE signal=LOW	Reset Alarm	
ALARM MUTE signal=HIGH		
	MIN	MAX
Logic level low voltage	0V	0.4V
Logic level high voltage	2.4V	5.25V

2.2.5. LED Indicators

These will be a bi-color LED to indicate power supply status.

Table 5 - LED indicators

Power supply condition	Power supply LED(s)
No AC power to all PSU	OFF
No AC power to this PSU only	Blinking Red
AC present /Only standby outputs on	Blinking Blue
Power supply DC outputs on and OK	Solid Blue
Power supply failure (includes over voltage, over temperature)	Solid Red
Fan fail or lock	
PWOK fail	
B/P-Fail	
Current limit	

The LED(s) shall be visible on the power supply’s exterior face. The LED location shall meet ESD requirements. LED shall be securely mounted in such a way that incidental pressure on the LED shall not cause it to become displaced.

2.3. DC Output Load Ratings

The system housing shall be capable of supplying the output current of table 6 subject to the list conditions and a total output power of up to **650W**. It is configured holding up to two identical power modules to achieve the redundancy. The maximum output current may vary depending on what power module will be utilized.

Table 6 –DC output load ratings

	+3.3V		+5V		+12V		-12V		+5VSB	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
650W	0.1A	24A	0.1A	30A	1A	52.9A	0A	0.5A	0.1A	4A
	Maximum combined power 170W.									
Maximum continuous total DC output power should not exceed 650W.										



Multi-output: (+3.3V, +5V, -12V)

2.3.1. Minimum Load Operation

The power supply shall meet all requirements except for the transient loading requirements when operated at min. load on all outputs.

2.3.2. Regulation

The power supply shall meet the regulation, ripple and noise limit under all operating conditions (AC line, transient loading, output loading). The regulation of Table 7 shall be measured at the output connector of the power supply, subject to the cross loading conditions in section 2.3

Table 7 – Output voltage regulation

Output	Output voltage limits(V_{ac})			
	Minimum	Nominal	Maximum	REG
+12V	11.40V	12V	12.60V	+/-5%
+5V	4.75V	5V	5.25V	+/-5%
+3.3V	3.135V	3.3V	3.465V	+/-5%
-12V	-10.8V	-12V	-13.20V	+/-10%
+5VSB	4.75V	5V	5.25V	+/-5%

2.3.3. Ripple and Noise

Ripple and noise shall be measured with 0.1uF of ceramic capacitance and 47uF of tantalum capacitance on each of the power supply output connector terminal. The ripple and noise shall be meet over all load ranges and AC line voltages. The output noise requirements shall apply over a 0Hz to 20MHz bandwidth.

Table 8 – Ripple and Noise

Output	+3.3V	+5V	+12V	-12V	+5VSB
Maximum ripple/noise	50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

2.3.4. Transient Response

The output voltages shall remain within the limits specified in 2.3.2 output rating table for the step loading and within the limits specified for the capacitive loading. The load transient repetition rate shall be tested between 50Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The step load may occur anywhere within the MIN load to the MAX load shown in Table 9.

Table 9: Transient Load Requirements

Output	Step Load Size	Load Slew Rate	Capacitive Load
+3.3V	30% of max load	0.5A/us	1000uF
+5V	30% of max load	0.5A/us	1000uF
+12V	50% of max load	1.0A/us	6600uF
+5VSB	25% of max load	0.5A/us	350uF



2.3.5. Output Voltage Rise Time

The turn on waveform for the main DC outputs shall be monotonic with less than 10% of overshoot.

2.3.6. Output Voltage Hold-up Time

Upon loss of input power, the outputs shall remain in regulation for at least 18msec.

2.3.7. Timing Requirements

The timing requirements for the ERP system housing's main outputs, 5VSB, and PWOK signal are defined for turn on and turn off of the power supply. The shut down timing requirements are also illustrated, for the current limit condition.

The timing of signals and power are specified in Table 10 and illustrated in Figure 1.

Table 10 - Turn on/off timing

Turn on	Description	Min	Max	Units
Tvout rise	Output voltage rise time from each main output		50*	msec
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation		1500	msec
Tac_on_delay	Delay from AC being applied to all output voltage being within regulation		2500*	msec
Tvout_holdup	Time all output voltages, including 5VSB, stay within regulation after loss of AC	18*		msec
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK	16*		msec
Tpson_on_delay	Delay from PSON [#] Active to output voltages within regulation limits	5	400	msec
Tpson_pwok	Delay from PSON [#] deactive to PWOK being deasserted		50	msec
Tpwok_on	Delay from output voltage within regulation limits to PWOK asserted at turn on	100	500*	msec
Tpwok_off	Delay from PWOK deasserted to main DC or 5VSB dropping out of regulation limits	1		msec
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal	100		msec



2.3.8. Timing Requirements Chart

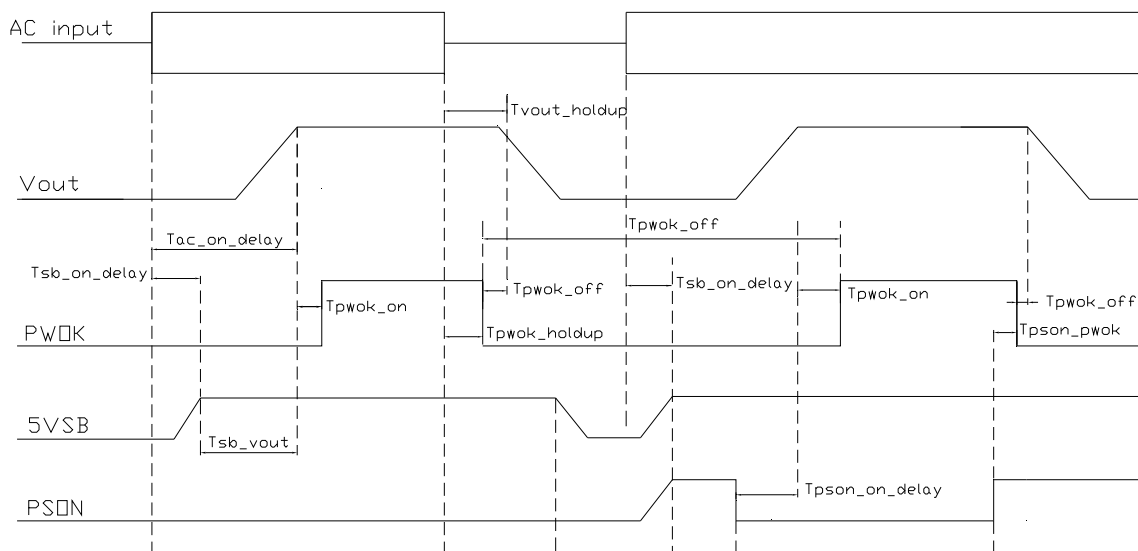


Figure 1 : Turn on/off timing

2.3.9. Overshoot

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 10mS.

2.3.10. Temperature Coefficient

After operating for 30 minutes or longer at 25° C ambient, the output voltages shall not change by more than $\pm 0.05\%$ per degree C for any given line and load conditions.

2.4. Protection Circuits

The 5VSB output shall remain on, if the failure does not involve this output. When a protection circuit shuts down the ERP both LEDs in the power module should indicate a fail and a PS_Alert signal shall be activated, if the power supply latches off due to a protection circuit tripping. An shut down of AC cycle for 15 sec and followed PS_ON cycle high for at least 1 sec shall reset the power supply.

2.4.1. Over Voltage Protection

Voltage Source	Protection Point
+3.3V	3.9V-4.8V
+5V	5.7V-6.5V
+12V	13.3V-15.6V



2.4.2. Over Current Protection

The ERP system housing has current limit to prevent the main outputs from exceeding the values shown in Table 11. If the current limits are exceeded, the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. +5VSB shall be protected under over current or shorted conditions so that no damage can occur to the power supply.

Table 11– Over current protection

Voltage	Over current limit
+12V/+5V/+3.3V	110% minimum; 150% maximum

2.4.3. Thermal Protection

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an over temperature condition the PSU shall be shutdown with the exception of the 5VSB output. The power supply shall alert the system of the OTP condition via the PS_ALERT signal and the fail LED indicator.

Sensor Type	Protect point		Recover point	
	MIN	MAX	MIN	MAX
Temp1 (ambient temp sensor)	55°C	60°C	50°C	55°C

2.5. Cooling and Smart Fan Speed

The power supply shall have two 40 x 20mm, ball bearing fans. Each fan shall have airflow of 18500rpm/20.1 CFM (maximum) with zero back pressure, pulling air out of the module.

Power mode	Fan working condition	Remark
No AC power to this PSU only	Fan PWM go 100% duty.	TBD
Power supply DC outputs on and OK	Fan PWM duty follow current mode and AMB temperature combine change.	TBD
AC present /Only standby outputs on	Fan PWM 100% duty start, normal mode at 50% duty.	TBD
Protection mode	Fan PWM go 100% duty.	Systematic temperature that it is overheated to take away at once.

2.6. Acoustic

Power	Standby mode	Power on mode										
		0%	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
650W	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	20Wmax	0W	65W	130W	195W	260W	325W	390W	455W	520W	585W	650W

Fan noise result at 1+1 redundant mode condition.

3. MECHANICAL

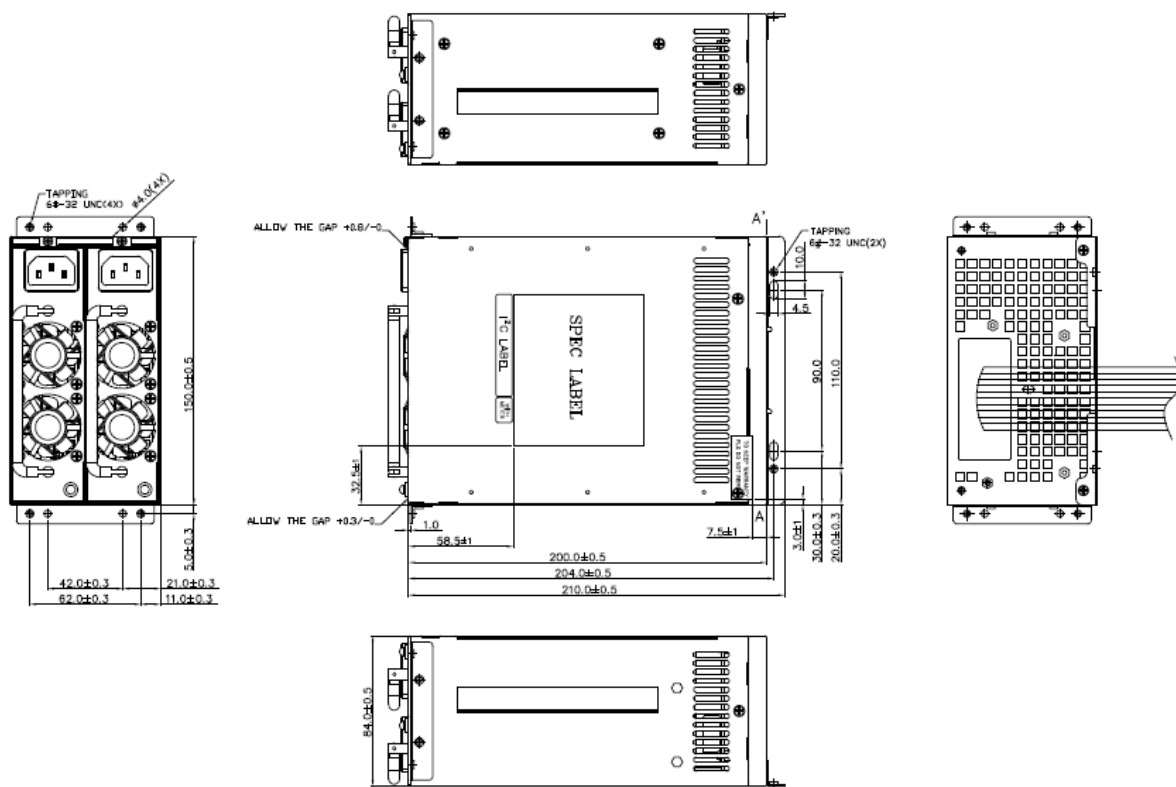
A metal enclosure holding the electrical backplane, which shall supply the main outputs and i2c



functionality to the system. The mechanical should be able to hold up to two power module, which lock into the mechanical outline. The mechanical outline should be mount able with brackets. Which can resist shock vibration test.

3.1. Dimension

The outside dimension, not including mounting brackets, handle and output connector, shall be W150mm x H84 mm x L200mm (without bracket length).

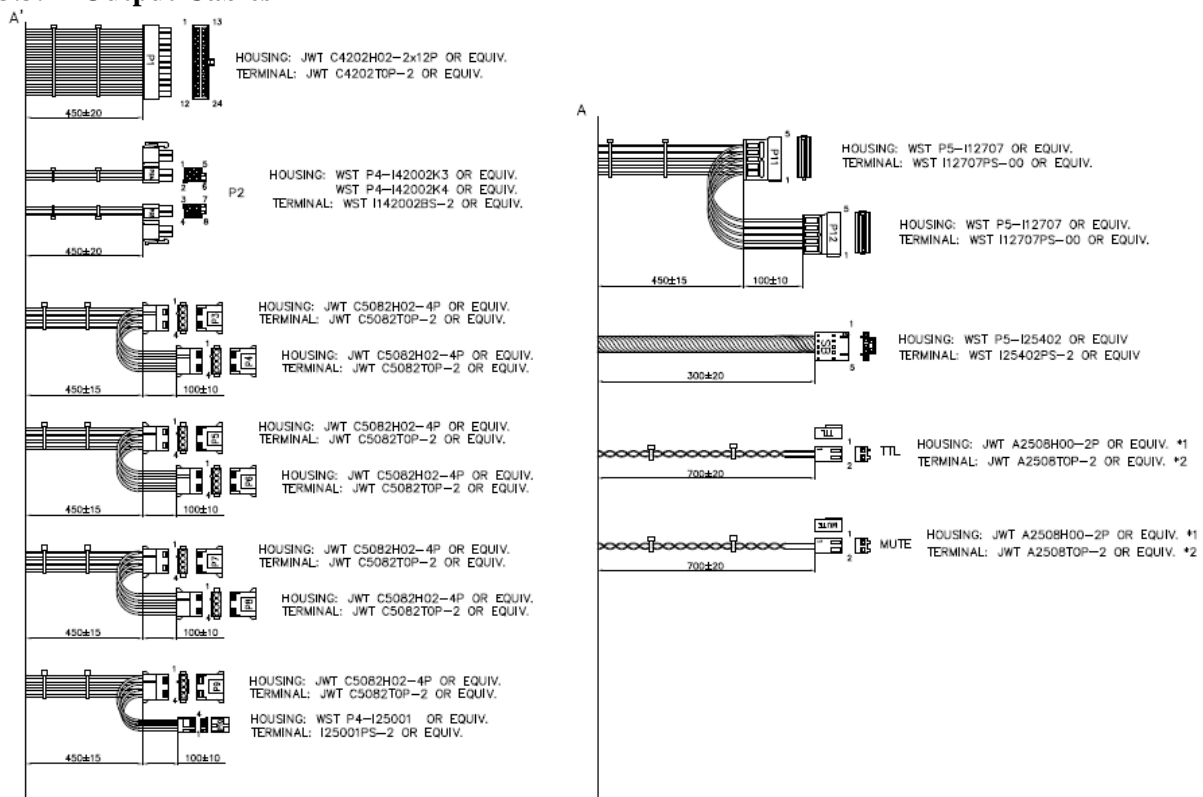


3.2. AC Input Connector

The power supply shall have an internal IEC320 C14 power inlet.



3.3. Output Cables



3.3.1 Output Pin Table

Do not recommend using extra connecting in series or connecting in parallel application by the power cables.

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P1	1	+3.3V	ORANGE UL1007 18AWG
	1	+3.3VS	ORANGE UL1007 22AWG
	2	+3.3V	ORANGE UL1007 18AWG
	3	GND	BLACK UL1007 18AWG
	4	+5V	RED UL1007 18AWG
	4	+5VS	RED UL1007 22AWG
	5	GND	BLACK UL1007 18AWG
	6	+5V	RED UL1007 18AWG
	7	GND	BLACK UL1007 18AWG
	8	PWOK(PG)	GRAY UL1007 24AWG
	9	+5VSB	PURPLE UL1007 18AWG
	10	+12V	YELLOW UL1007 18AWG
	10	+12VS	YELLOW UL1007 22AWG
	11	+12V	YELLOW UL1007 18AWG
	12	+3.3V	ORANGE UL1007 18AWG
	13	+3.3V	ORANGE UL1007 18AWG
	14	-12V	BLUE UL1007 18AWG
	15	GND	BLACK UL1007 18AWG
	16	PSON	GREEN UL1007 24AWG
	17	GND	BLACK UL1007 18AWG
	18	GND	BLACK UL1007 18AWG
	19	GND	BLACK UL1007 18AWG
	20		
	21	+5V	RED UL1007 18AWG
22	+5V	RED UL1007 18AWG	
23	+5V	RED UL1007 18AWG	
24	GND	BLACK UL1007 18AWG	

PIN NUM	PIN CONN	COLOR	WIRE TYPE
P2 (P2A+ P2B)	1	GND	BLACK UL1007 18AWG
	2	GND	BLACK UL1007 18AWG
	3	GND	BLACK UL1007 18AWG
	4	GND	BLACK UL1007 18AWG
	5	+12V	YELLOW UL1007 18AWG
	6	+12V	YELLOW UL1007 18AWG
	7	+12V	YELLOW UL1007 18AWG
	8	+12V	YELLOW UL1007 18AWG

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P3	1	+12V	YELLOW UL1007 18AWG
	2	GND	BLACK UL1007 18AWG
P5	1	+12V	YELLOW UL1007 18AWG
	2	GND	BLACK UL1007 18AWG
P7	1	+12V	YELLOW UL1007 18AWG
	2	GND	BLACK UL1007 18AWG
P9	1	+12V	YELLOW UL1007 18AWG
	2	GND	BLACK UL1007 18AWG

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P4 P6 P8	1	+12V	YELLOW UL1007 18AWG
	2	GND	BLACK UL1007 18AWG
	3	GND	BLACK UL1007 18AWG
	4	+5V	RED UL1007 18AWG

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P10	1	+5V	RED UL1007 22AWG
	2	GND	BLACK UL1007 22AWG
	3	GND	BLACK UL1007 22AWG
	4	+12V	YELLOW UL1007 22AWG

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P11 P12	1	+12V	YELLOW UL1007 18AWG
	2	GND	BLACK UL1007 18AWG
	3	+5V	RED UL1007 18AWG
	4	GND	BLACK UL1007 18AWG
	5	+3.3V	ORANGE UL1007 18AWG

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
SB	1	I ² CSCL	GRN/WHT UL1007 24AWG
	2	I ² CSDA	YEL/WHT UL1007 24AWG
	3	PS-Alert	WHITE UL1007 24AWG
	4	GND	BLACK UL1007 24AWG
	5		

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
TTL	1	GND	BLACK UL1007 24AWG
	2	TTL SIGNAL	RED UL1007 24AWG

PIN NUM	PIN CONN	COLOR	WIRE SPEC.
MUTE	1	GND	BLACK UL1007 24AWG
	2	ALARM MUTE	YELLOW UL1007 24AWG



4. ENVIRONMENTAL

The power supply shall operate normally, sustain no damage as a result of the environmental conditions listed in paragraphs 4.1 through 4.6.

4.1. Temperature

A) Operating: The operating ambient temperature for max. rated loading shall be 0°C to 50°C at module inlet. The maximum rate of temperature delta shall be 5°C/10 minutes, but shall not exceed 10°C/hour.

B) Storage (non-operating): The non-operating ambient temperature shall be -40°C to 70°C. Maximum rate of change shall be 2°C/minute.

4.2. Humidity

The operating humidity shall be limited to 85% relative humidity non-condensing, over the rated operating temperature range. The power supply shall operate at full load under these conditions.

The non operating humidity shall be limited to 95%relative humidity, non-condensing.

4.3. Altitude

A) Operation : sea level to 16,400 feet.

B) Non-Operation : sea level to 50,000 feet.

4.4. Vibration

A) Operation : 0.01G²/Hz at 10Hz, 0.02G²/Hz at 20Hz.

B) Non-Operation : 0.02G²/Hz form 20Hz to 1000Hz.

4.5. Thermal shock

The thermal shock -40°C to +70°C, non-operating, 10 cycles, transfer time shall not exceed 5 minutes, duration of exposure to temperature extremes shall be 20 minutes.

4.6. Shock

A) Operation : 5G no malfunction.

B) Non-Operation : 50G no damage.

4.7. Power Line Disturbance

4.7.1. AC Line Transient Specification

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Line Sag

AC Line Sag				
Duration	Sag	Operating AC voltage	Line frequency	Performance criteria
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 16ms	100%	Nominal AC voltage	50/60Hz	No loss of function or performance
>17 ms	>10%	Nominal AC voltage	50/60Hz	Loss of function acceptable, self recoverable



Line Surge

AC Line Surge				
Duration	Surge	Operating ac voltage	Line frequency	Performance criteria
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

4.7.2. AC Line Fast Transient Specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the level 3 requirements for surge-withstand capability, with the following conditions and exception:

- These input transients shall not cause any out-of-regulation conditions, such as overshoot and undershoot, nor shall they cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test shall not produce damage to the power supply.
- The supply shall meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

5. REGULATORY

5.1. Agency Requirements

- A) UL 60950-1.
- B) cUL
- C) TUV EN60950-1.
- D) CB Report.
- E) European Union CE Marking

5.2. Maximum AC Leakage Current to Ground

3.5mA max at 240Vac

5.3. Electromagnetic compatibility

5.3.1. EMI/EMC Requirements

- A) EMI, RFI:
CISPR CLASS B.
Shall have a minimum of 3dB margin.
- B) IMMUNITY:
IEC61000-4-2
IEC61000-4-2
IEC61000-4-3
IEC61000-4-4
IEC61000-4-5

6. Power Supply Management

6.1. Hardware Layer

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 “high power” and I2C Vdd based power and drive specification.



This bus shall operate at 3.3V but be tolerant to 5V pull-ups. The power supply should not have any internal pull-ups on the SMBus, pull-ups shall be located on system side.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0, A1 and A2 on the power supply module. The circuits inside the power supply shall derive their 3.3V power from the 5Vsb bus through a buffer. Device(s) shall be powered from the system side of the 5VSB or 'ring device. No pull-up resistors shall be on SCL or SDA inside the power supply. The pull-up resistors should be located external to the power supply on system/application side.

6.2. Capacitance for SMBus

The recommended Capacitance per pin on SDA and SCL shall be 10pF, and is not allowed to exceed 40pF per pin. In an N+1 configuration of up to eight (8) power modules with additional PDB, the total Capacitance of each Bus pin shall not exceed 400pF.

6.3. I2c Bus noise requirement

The power supplies i2c bus' SDA and SCL line shall be clean from noise, which might affect the proper function when utilized with other devices.

The maximum allowed line noise on SDA or SCL is 300Mv@100MHZ.

6.4. Pull Ups

The main pull-ups are provided by the system and may be connected to 5V or 3.3V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail. In case the power supply requires pull-ups internal, the pull up resistance shall be very weak on SDA or SCL.

6.5. Power Supply Management Controller (PSMC)

The PSMC device on the PDB shall derive its power of the 5Vsb output on the system side of the O'ring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2

It shall be located at the address set by the A0, A1 and A2 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

Table 12 – PSMC Addressing for inserted power modules

PDB position and PSMC address		PM1 B0h/B1h	PM2 B2h/B3h	PDB 4Ah/4Bh
Pin	A2/A1/A0	0/0/0	0/0/1	None

6.6. Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General



Requirements, Transport And Electrical Interface; Revision 1.2

- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2
- System Management Bus (SMBUS) Specification 2.0

6.7. Data Speed

The PSMC device on the PDB shall operate at the full 100kbps (100kHz) SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply is allowed to clock stretch while parsing a command or servicing multiple interrupts or NACK.

Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

The PSMC may support 400kbps (400kHz) PMBus speed.

6.8. Bus Errors

The PSMC shall support SMBus clock-low timeout (T_{timeout}). This capability requires the PSMC to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions within 10ms later. The total reset time from detection of the condition till restarted, ready to receive commands condition shall not exceed 35ms.

The device must recognize SMBus START and STOP conditions on ANY clock interval. The PSMC must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup. Or hold times that are shorter than the minimums specified by the SMBus specifications. The PSMC is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the PSMC 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and NACK. The PSMC is supposed to re-synch with the master on the next START or STOP condition.

6.9. General Call Address

The PSMC shall respond to the General Call Address (00h) as well to its own physical address.

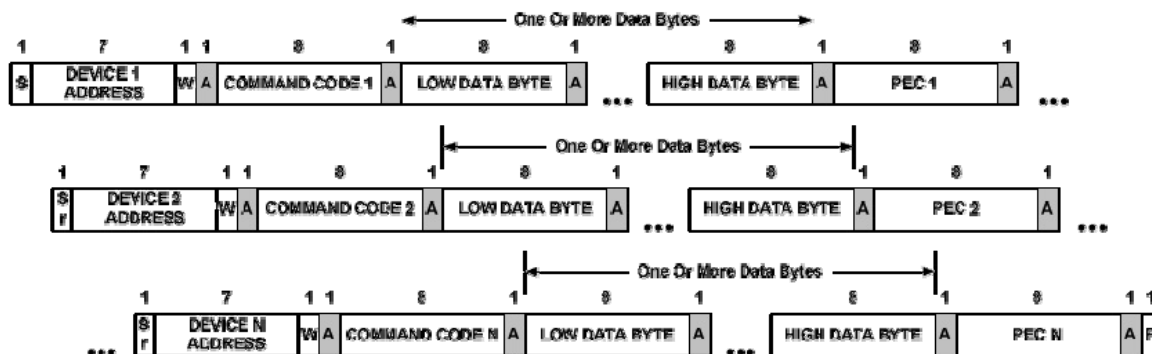
6.10. Group Command

The Group Command is used to send commands to more than one PMBus device at a time. The commands are sent in one continuous transmission. When the PSMC detect the STOP condition that ends the sending of commands, it shall begin executing the command which it received or NACK, if the command is not supported.

The Group Command Protocol is not allowed to be used with commands that require the PSMC to respond to the data (only WRITES).



Figure 3 – Group Command with PEC



6.11. Extended Command

The Extended Command protocol allows for an extra 256 command codes. This command is similar to the Block-Write/Block-Read Word process call in the SMBus Specification, but allows an maximum length of 256 command codes. The first byte (the low data byte) is a reserved value indicating that the extended command format is being used. The second byte (the high order byte) is the command to be executed. This allows the standard commands to be extended by PMBus and Manufacture specific commands.

Command Extension Codes:

1. MFR_SPECIFIC_COMMAND EXT: FEh
2. PMBUS_COMMAND EXT: FFh

Please see below illustration for utilization:

Figure 4 – Extended Command Write

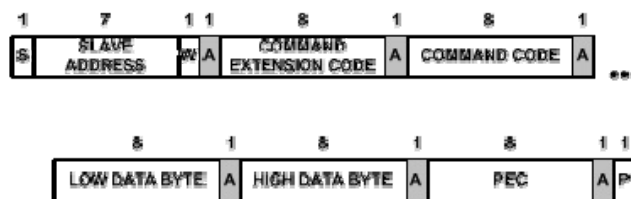
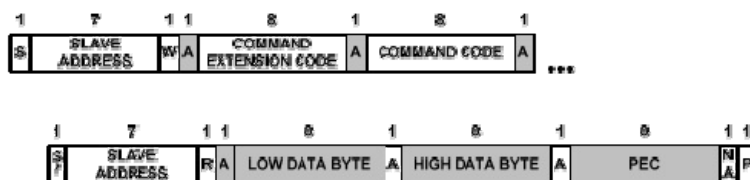


Figure 5 – Extended Command Read



6.12. Firmware Updates

The PSMC shall support firmware updates over the SMBus. In order to perform Firmware Updates, the WP needs to be pulled low and appropriated Software tool are required to guaranty the successful update.



6.13. Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be meet at the specified environmental condition and the full range of rated input voltage.

Table 13 – Sensor Accuracy

Sensor	10% - 20% load	> 20% - 50% load	> 50% - 100% Load
Current	± TBD%	± TBD%	± TBD%
Voltage	± 5%	± 5%	± 5%
Temperature	± 3°C with Δ5%		
FAN	Provided by the power module		
Input Power	± 15%	± 5%	± 5%
	Provided by the power module		

6.14. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose.

All Sensors shall continue to provide real time data as long as the PSMC device is powered. This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 14 – PSMC Sensor list

Sensor	Description
V_{input}	Input Voltage
I_{input}	Input Current
P_{input}	Input Power
$V_{output\ main}$	Output Voltage main output
$I_{output\ main}$	Output Current main output
$P_{output\ main}$	Output Power main output
$V_{output\ aux}$	Output Voltage auxiliary output
$I_{output\ aux}$	Output Current auxiliary output
$P_{output\ aux}$	Output Power auxiliary output
T_{comp}	Component Temperature
T_{env}	Environmental Temperature
PDB_{fail}	PDB fail protection

6.15. Power Supply Field Replacement Unit (FRU)

The PDB shall support electronic access of FRU information over an I²C bus. Five pins at the power supply connector are allocated for this. They are named SCL, SDA, A0, A1, and A2. SCL is serial clock. SDA is serial data. These two bidirectional signals are from the basic communication lines over the I²C bus. A0, A1, and A2 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I²C address shall be per table below.



The device used for this shall be powered from a 5V bias voltage derived from the 5 VSB output on the system side of the O-ring device. No pull-up resistors shall be on SCL or SDA inside the power supply.

The write control (or write protect) pin shall be tied to ground inside the power supply so that information can be written to the EEPROM. A0, A1, and A2 shall be pulled high inside the power supply to the EEPROM bias voltage through separate resistors.

Table 15 - EEPROM Addressing

PDB position and FRU address	PM1 A0h	PM2 A2h/A3h	PDB ACh/ADh
Pin A2/A1/A0	0/0/0	0/0/1	None

6.16. FRU Data

The FRU Data format shall be compliant with the IPMI ver. 1.0 (per rev. 1.1 from Sep.25th, 1999) specification. The current version of this specification is available at <http://developer.intel.com/design/servers/ipmi/specs.htm>. The following is the exact listen of the EEPROM content. During testing this should be followed and verified.

6.17. FRU Device protocol

The FRU device will implement the same protocols as the commonly used ATC24C02 device, including Byte Read, Sequential Read, Byte Write, and Page Read protocols.

6.18. FRU Data Format

The information to be contained in the FRU device is shown in the following table.

Table 16 - EEPROM Addressing

<u>Area Type</u>	<u>Description</u>
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document. Product information shall be defined as follows:
<u>Field Name</u>	<u>Field Description</u>
Manufacturer Name	3Y Power
Product Name	YH5651-1TA02R
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	TBD
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}
Multi-Record Area	As defined by the IPMI FRU document. The following



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	record types shall be used on this power supply: - Power Supply Information (Record Type 0x00) DC Output (Record Type 0x01) No other record types are required for the power supply. Multi-Record information shall be defined as follows:
Field Name (PS Info)	Field Information Definition
Overall Capacity (watts)	650
Peak VA	850
Inrush current (A)	55
Inrush interval (msec)	TBD
Low end input voltage range 1	90
High end input voltage range 1	132
Low end input voltage range 2	180
High end input voltage range 2	264
A/C dropout total. (msec)	15
Binary flags	Set for: Hot Swap support, Auto switch, and PFC
Peak Wattage	Set for: 725 Watts
Combined wattage	650
Predictive fail Tach support	Supported
Field Name (Output)	TBD
Output Information	TBD
All other output fields	Format per IPMI specification, using parameters in this specification.

The serial bus communication devices for PSMI data in the power supply shall be compatible with both SMBUS and I2C Vdd based power and drive. This bus shall operate at 5V bus The SMBUS pull-ups are located on the motherboard and may be connected to 5V.

Two pins are allocated on the power supply. One pin is the serial clock (PSM clock). The second pin is used for serial data (PSM data). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their power from the 5VSB bus. Device(s) shall be powered from the system side of the 5VSB or'ing device. No pull-up resistors shall be on SCL or SDA inside the power supply. There pull-up resistors should be located external to the power supply.



7. MISCELLANEOUS

7.1. Marking

7.1.1. Model label

Please refer to PLM system and check the label part number as below:

6LL13797XXGP

Label PN

Label Rev.

Rohs Parts

7.2. Reliability

The mean time between failure figure, calculated per BELL CORE TR-322 at 25 °C ambient, nominal AC input and maximum load, shall be at least 100,000 hours excluding fan MTBF, and 50,000 hours including fan MTBF.

8. RESTRICTION OF HAZARDOUS SUBSTANCE (ROHS) IN ELECTRICAL

The directive 2002/95/EC of the European Parliament and of the Council of the 27th January 2003, on the restriction of the use of certain hazardous substances in electrical and electronic equipment, requires the reduction of the substances Lead, Mercury, Cadmium, Hexavalent Chromium, Polybrominated Biphenyls (PBB), and Polybrominated Diphenyl Ethers (PBDE) in electronic products by July 1, 2006. Unless otherwise noted, all materials used will be compliant with this directive and any subsequent revisions or amendments.

